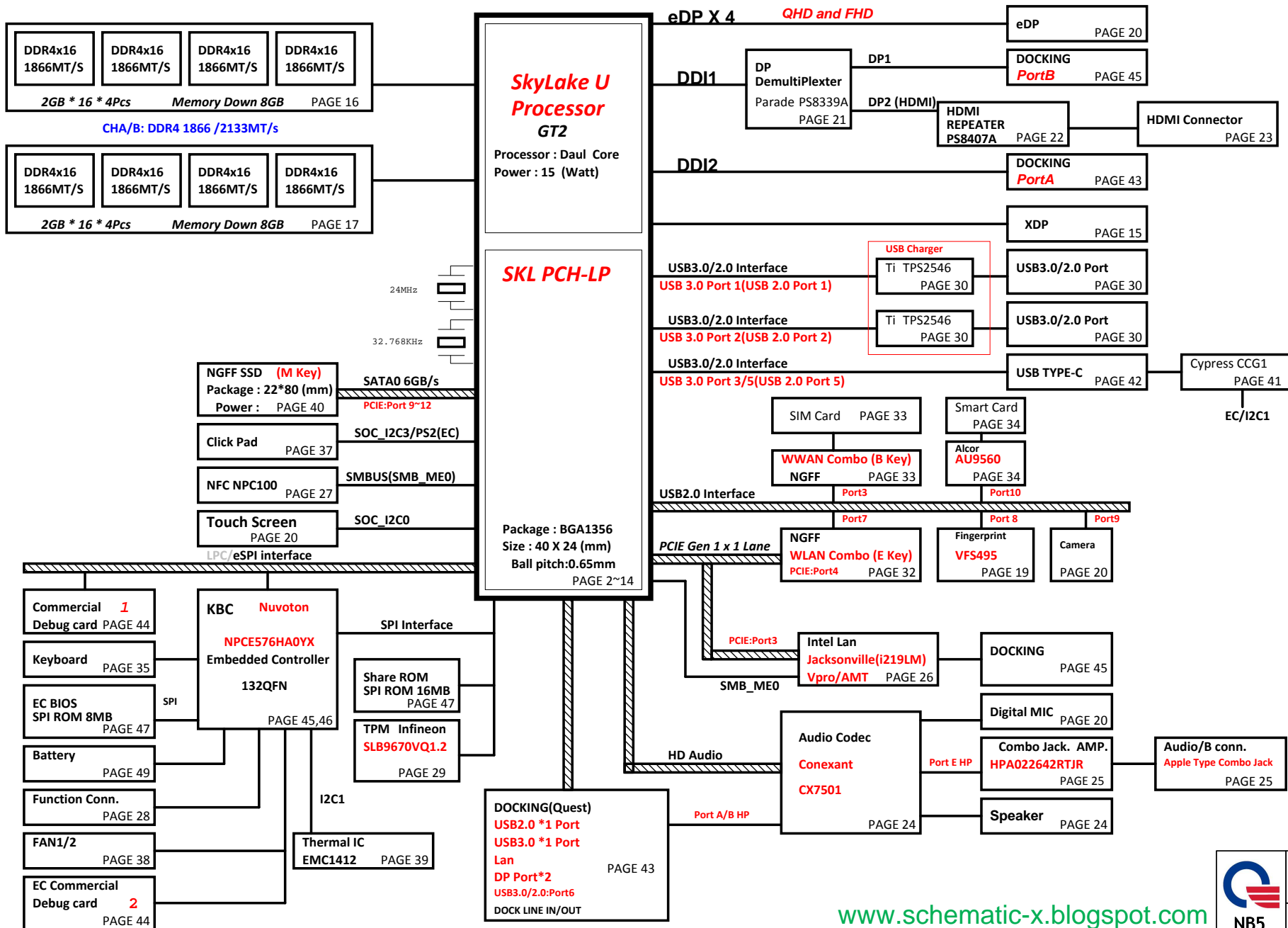


# 2015 Bellagio 1.0, Y0F ,14"UMA Schematics

PCB 10L STACK UP(1.0mm)

01

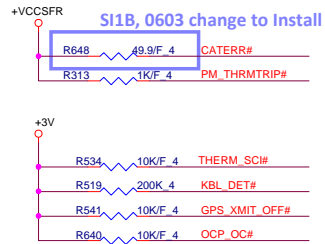
LAYER 1 : TOP  
LAYER 2 : SGND  
LAYER 3 : IN1(High)  
LAYER 4 : IN2(High)  
LAYER 5 : SGND  
LAYER 6 : SVCC  
LAYER 7 : IN3(High/Low)  
LAYER 8 : IN4(HIGH)  
LAYER 9 : SGND  
LAYER 10 : BOT



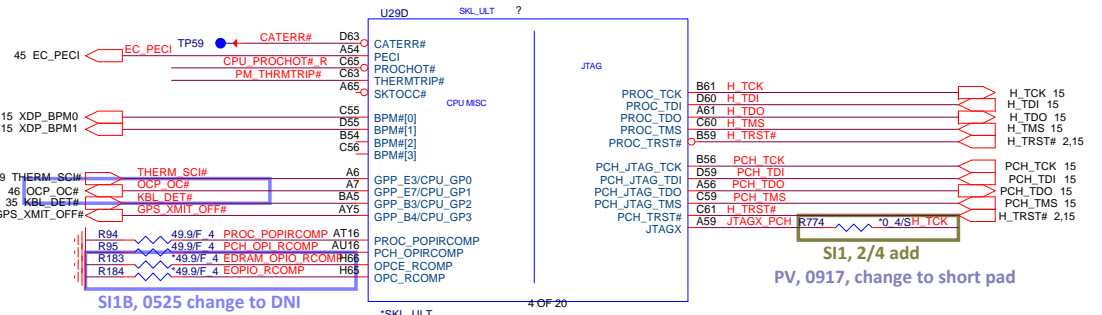
www.schematic-x.blogspot.com

**PROJECT : Y0F**  
**Quanta Computer Inc.**

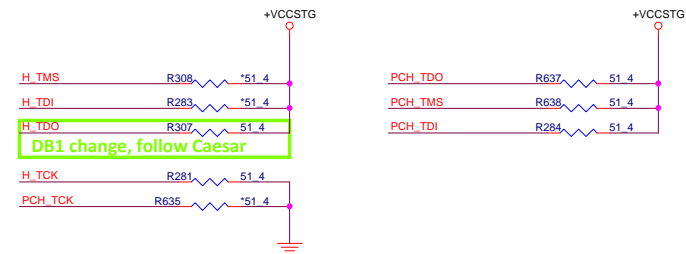
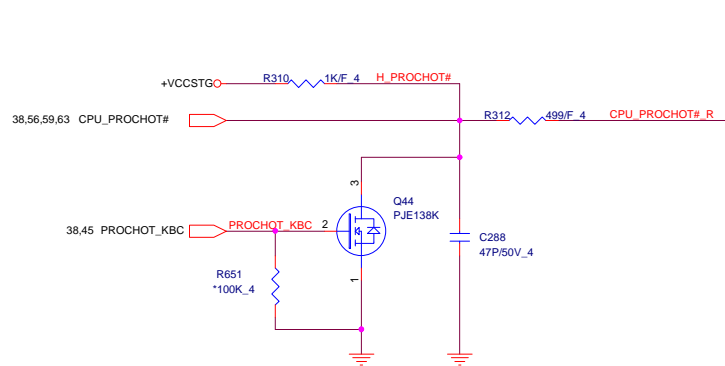
Size Custom Document Number Block Diagram Rev 1A  
Date: Tuesday, December 29, 2015 Sheet 1 of 67




**SI1B, 0528 change to GPP\_E7**

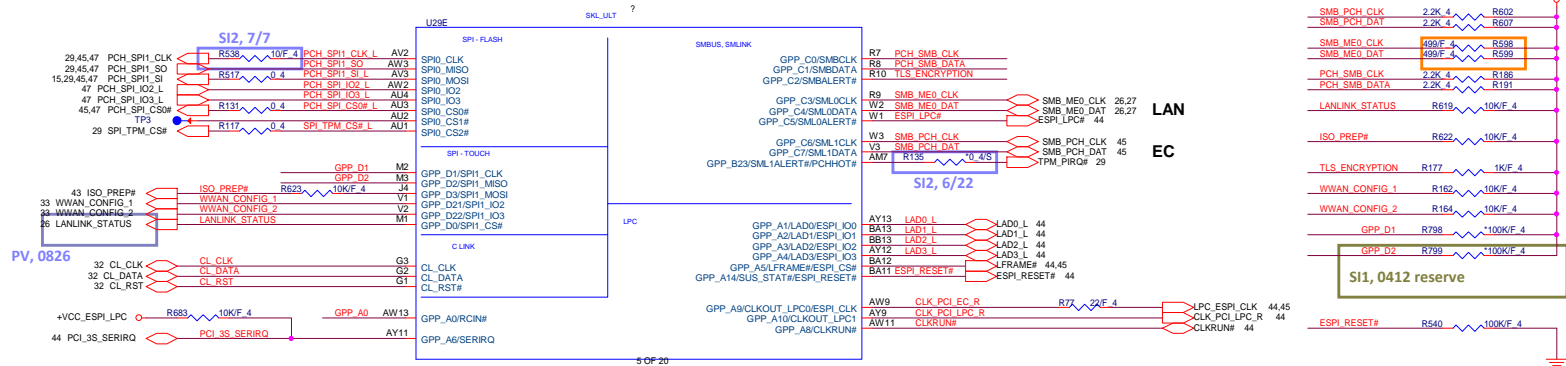


### Processor pull-up (CPU)



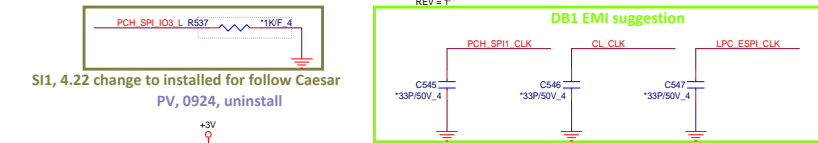
+VCCSTG 11,13,62  
 +VCCSFR 3,11,13,45,56,59,62  
 +3V 3,4,5,7,8,9,10,15,19,20,21,22,24,27,28,29,37,38,39,40,44,45,48,49,56,62,64

 <b>NB5</b>	<b>PROJECT : Y0F</b> <b>Quanta Computer Inc.</b>		
	Size Custom	Document Number <b>SKYPAKE (MISC/JTAG)</b>	Rev 1A
Date: Tuesday, December 22, 2015		Sheet 2 of 67	

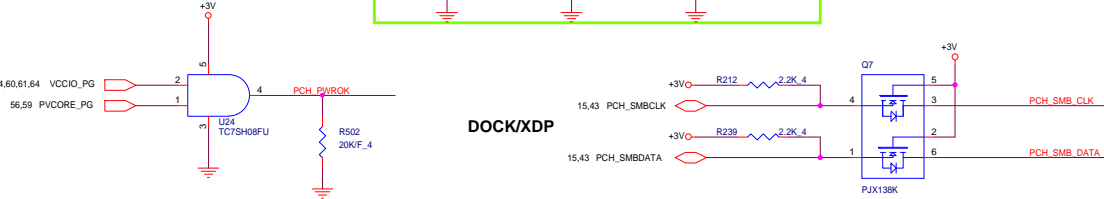


03

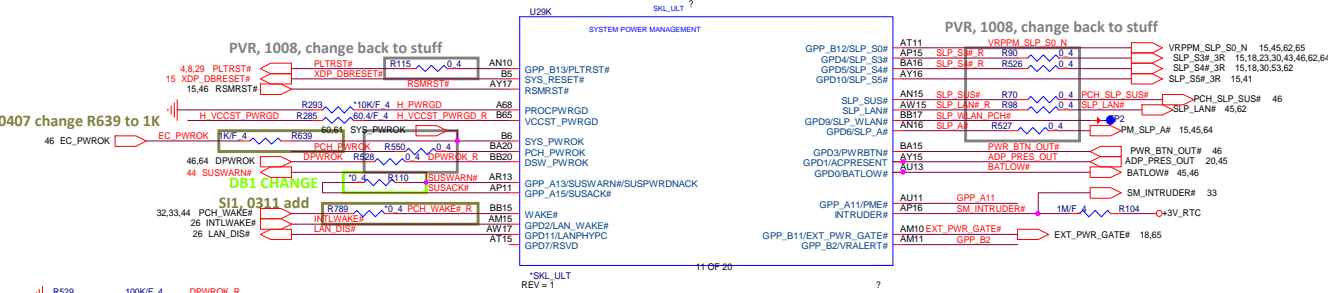
Follow 544506  
I219 Schematic  
and Layout  
Checklists v0.7  
suggestion to  
change to  
499ohm



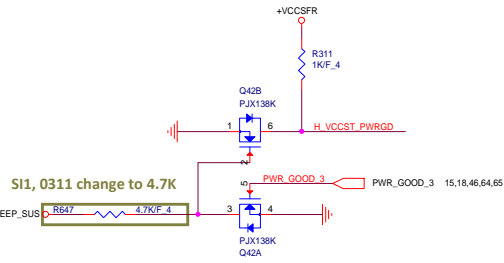
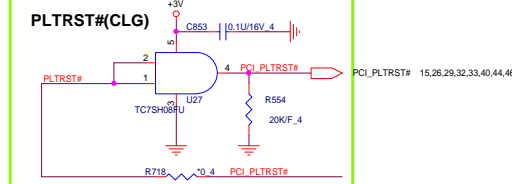
DOCK/XDP



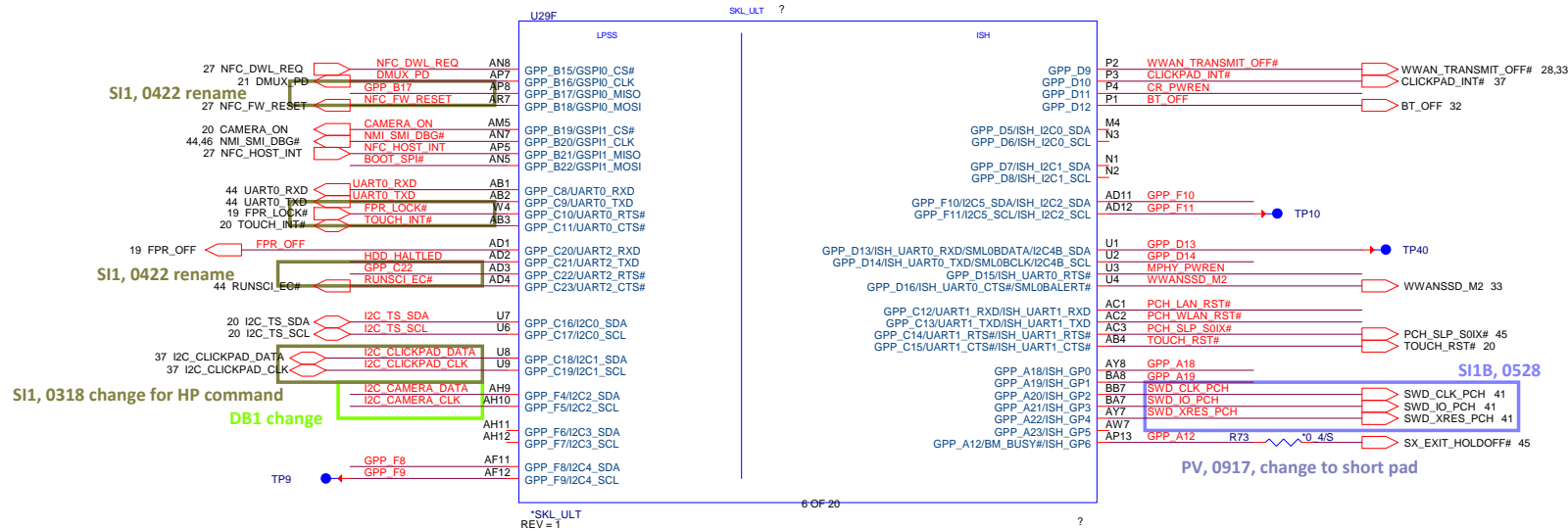
PCH Pull-high/low(CLG)



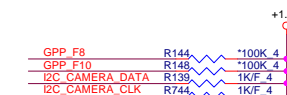
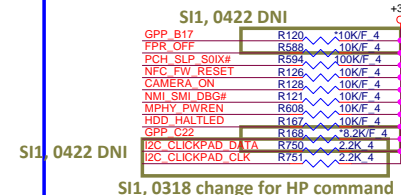
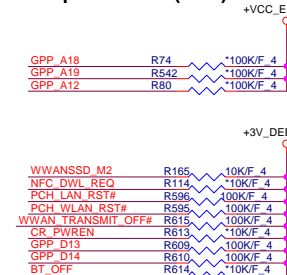
DB1 CHANGE



## Skylake (GPIO)



## GPIO Pull-up/Pull-down(CLG)



Signal	Usage	When Sampled	Comment
SPKR / GPP_B14	Top Swap Override	Rising edge of PCH_PWROK	<p>The signal has a weak internal pull-down. 0 = <b>Disable</b> "Top Swap" mode. (Default) 1 = <b>Enable</b> "Top Swap" mode. This inverts an address on access to SPI and firmware hub, so the processor believes it fetches the alternate boot block instead of the original boot-block. PCH will invert A16 (default) for cycles going to the upper two 64-KB blocks in the FWH or the appropriate address lines (A16, A17, or A18) as selected in Top Swap Block size soft strap.</p> <p><b>Notes:</b></p> <ol style="list-style-type: none"> <li>The internal pull-down is disabled after PLTRST# de-asserts.</li> <li>Software will not be able to clear the Top Swap bit until the system is rebooted.</li> <li>The status of this strap is readable using the Top Swap bit (Bus0, Device31, Function0, offset DCH, bit4).</li> <li>This signal is in the primary well.</li> </ol>
GSPI0_MOSI / GPP_B18	No Reboot	Rising edge of PCH_PWROK	<p>The signal has a weak internal pull-down. 0 = <b>Disable</b> "No Reboot" mode. (Default) 1 = <b>Enable</b> "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.</p> <p><b>Notes:</b></p> <ol style="list-style-type: none"> <li>The internal pull-down is disabled after PLTRST# de-asserts.</li> <li>This signal is in the primary well.</li> </ol>
SMBALERT# / GPP_C2	TLS Confidentiality	Rising edge of RSMRST#	<p>This signal has a weak internal pull-down. 0 = <b>Disable</b> Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default) 1 = <b>Enable</b> Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.</p> <p><b>Notes:</b></p> <ol style="list-style-type: none"> <li>The internal pull-down is disabled after RSMRST# de-asserts.</li> <li>This signal is in the primary well.</li> </ol>

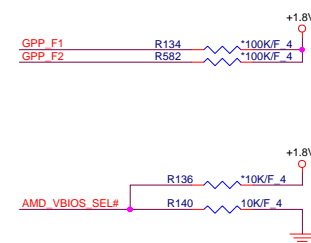
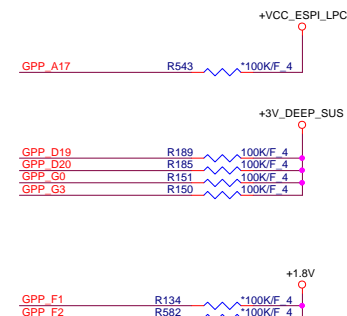
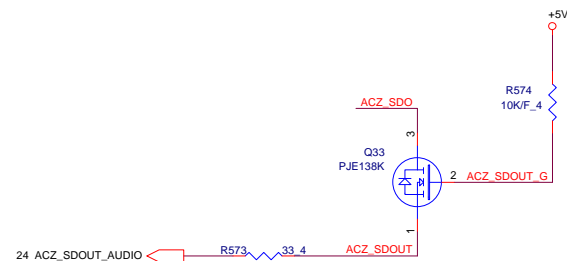
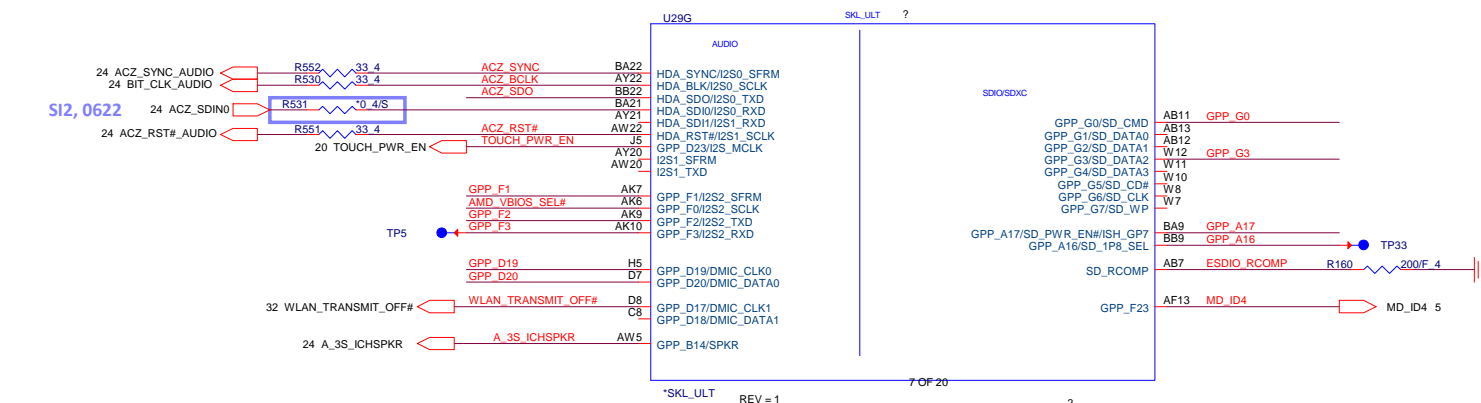
1.8V 5.8,24,64,65  
 3VPCU 3.10,15,18,27,28,30,32,33,35,36,39,41,43,44,45,46,47,48,49,50,51,52,53,54,55,60,61,62,63,64,65,66  
 3V\_DEEP\_SUS 3.5,6,8,10,15,18,27,32,37,44,45,47,52,54,55,62,64,65  
 3V 2.3,5,7,8,9,10,15,19,20,21,22,24,27,28,29,37,38,39,40,44,45,48,49,56,62,64



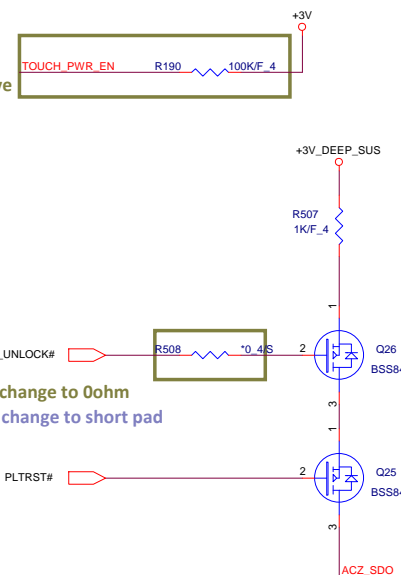








SI1, 0424 remove



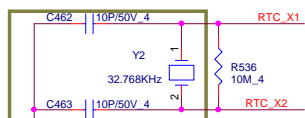
SI1, 0421 change to 0ohm

PV, 0917, change to short pad

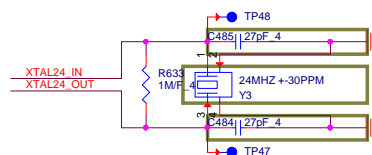




## RTC Clock 32.768KHz



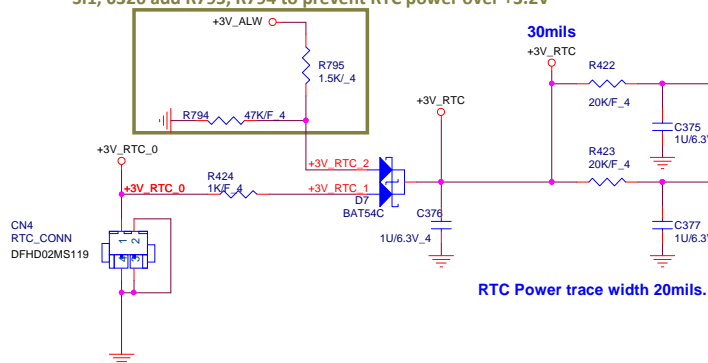
SI1, 0326 change Y2 to CL 9pF type and change C462 to 10p, C463 to 10p as vender recommend



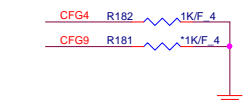
SI1, 0428 change to 24M to CL 20p, follow for Intel DG

## RTC Circuitry(RTC)

SI1, 0326 add R795, R794 to prevent RTC power over +3.2V

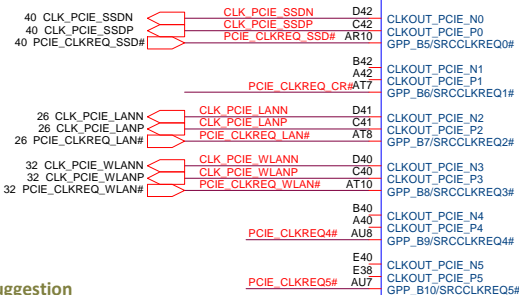


RTC Power trace width 20mils.



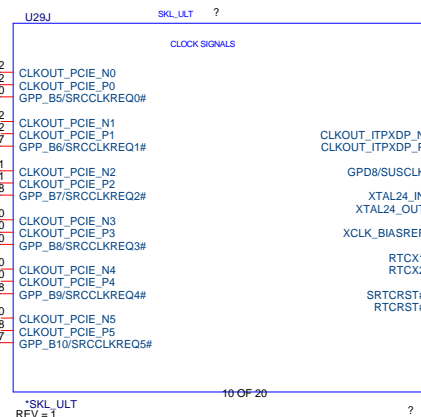
+VCCSFR 2,3,11,13,45,56,59,62  
+1.0V\_DEEP\_SUS 10,15,52,55,62,65  
+3V 2,3,4,5,7,8,10,15,19,20,21,22,24,27,28,29,37,38,39,40,44,45,48,49,56,62,64

SSD

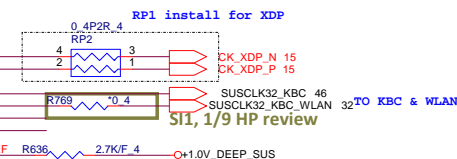


LAN

WLAN

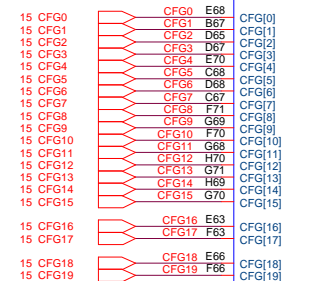


TBT

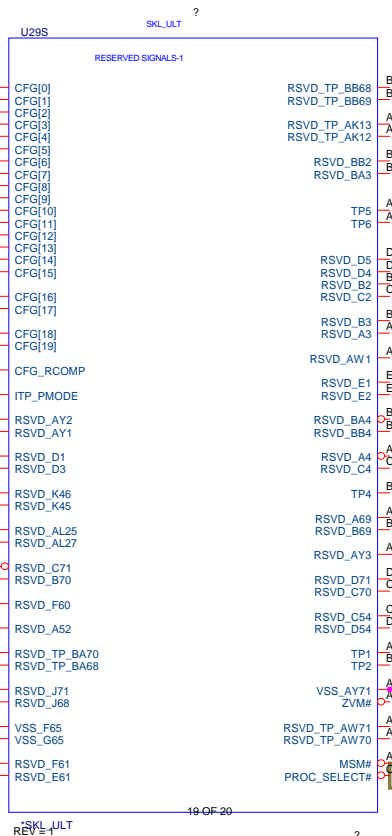


SI1, 3/18 Del for don't need reserve for Cannon Lake, support Kaby lake

CFG0-19 need Reserve TP



+1.0V\_DEEP\_SUS 15 ITP\_PMODE

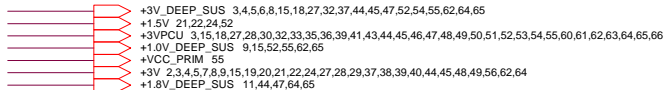


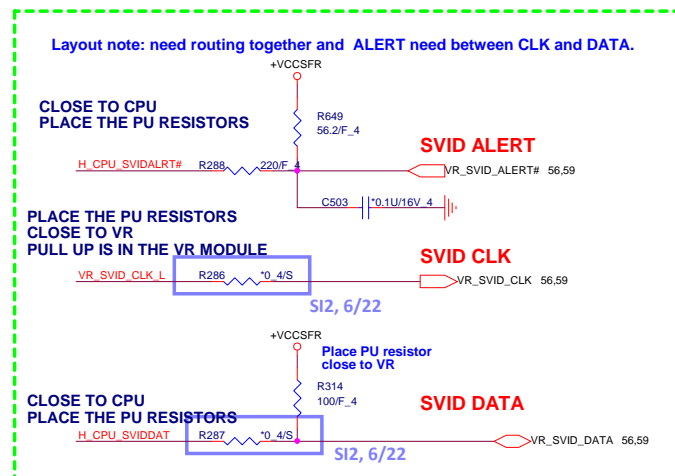
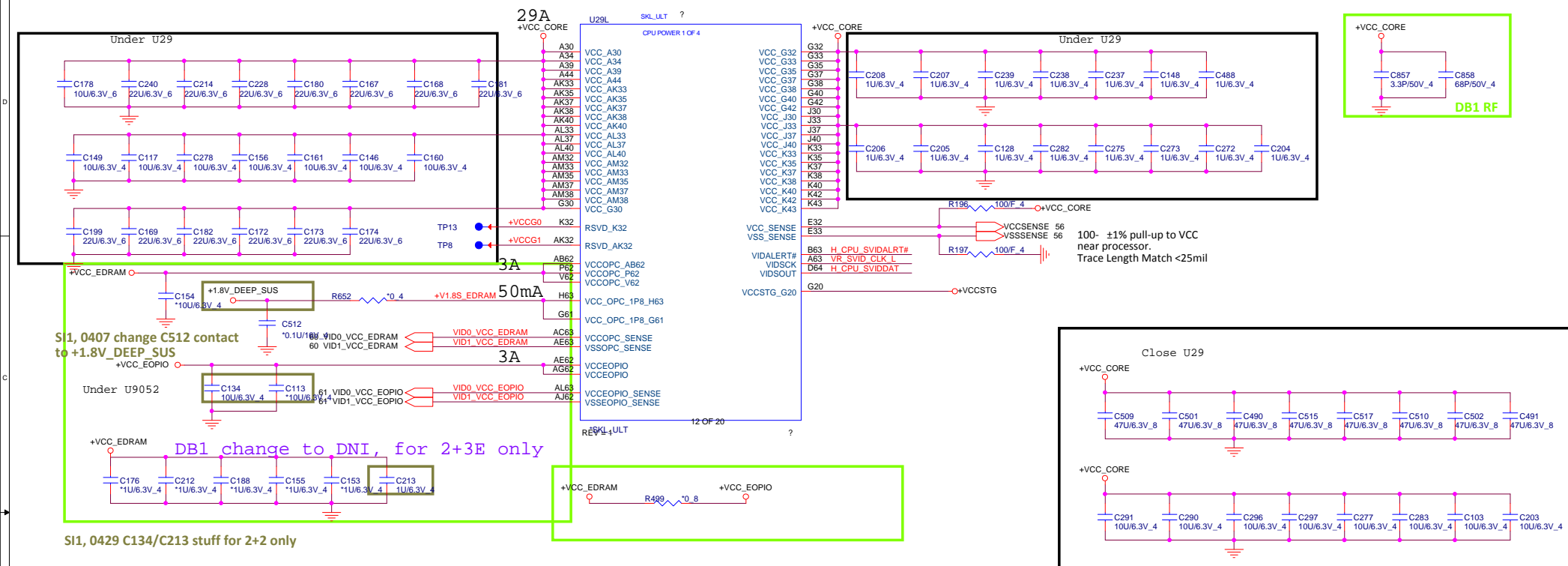
CLK\_REQ/Strap Pin(CLG)

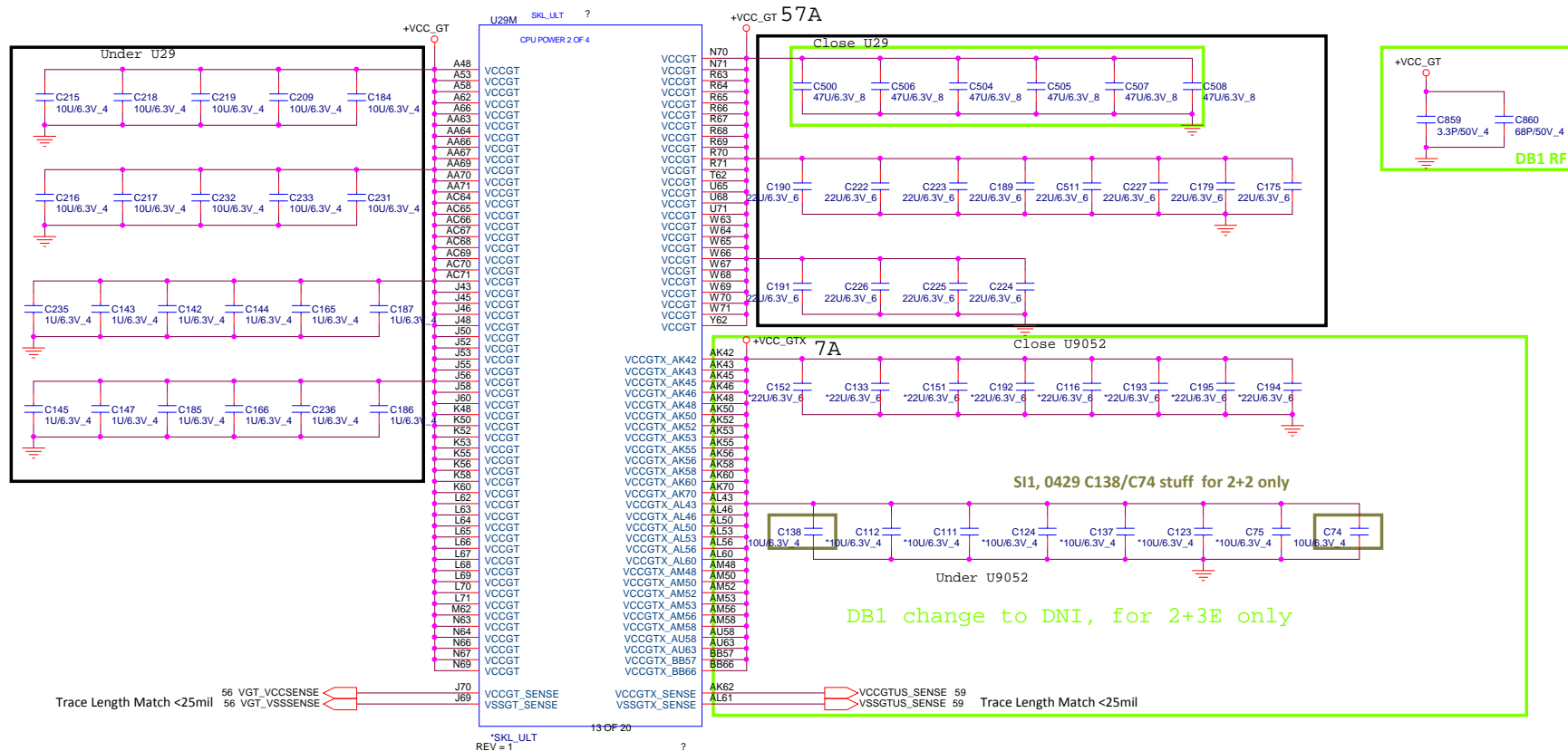


SI1, 3/18 Del for don't need reserve for Cannon Lake, support Kaby lake

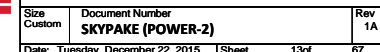
SI1, 3/18 Del for don't need reserve for Cannon Lake, support Kaby lake





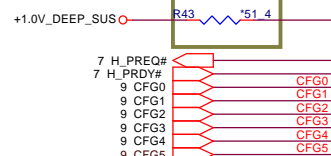


+VCC\_GT 56,58  
+VCC\_GTX 59





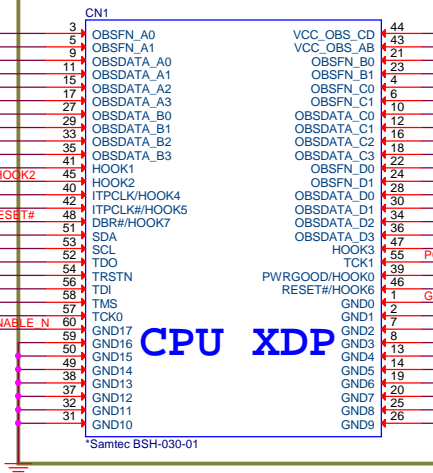
## SI1, 2/4 change to DNI



## SI1B, 0521

15,36,43,46 ON\_OFF#1\_Q

## SI1, 3/26 Correct XDP pin define



+1.0V\_DEEP\_SUS

+1.0V\_DEEP\_SUS

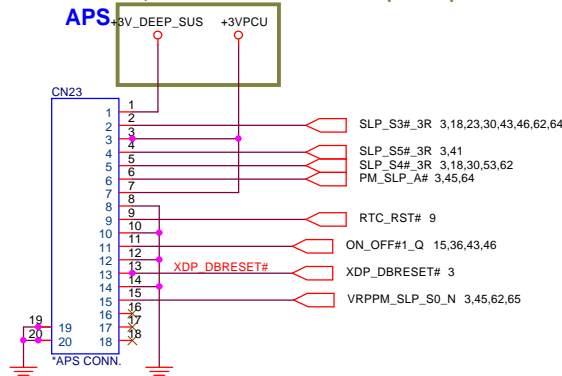
## CPU XDP

SI1, 4/13 change to 0201 type for ME concern  
PV, 0917, change to short pad

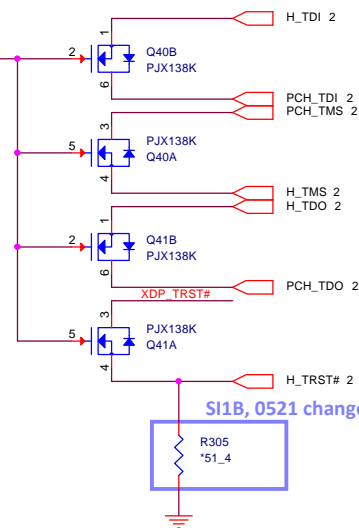
GND0 1K/F 4 R42 CFG3

## SI1, 0422 corrected APS conn. power pin define

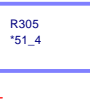
## APS



3,18,46,64,65 PWR\_GOOD\_3



## SI1B, 0521 change to DNI



+3V\_DEEP\_SUS 3,4,5,6,8,10,18,27,32,37,44,45,47,52,54,55,62,64,65

+1.0V\_DEEP\_SUS 9,10,52,55,62,65

+VCC\_IO 5,13,38,54

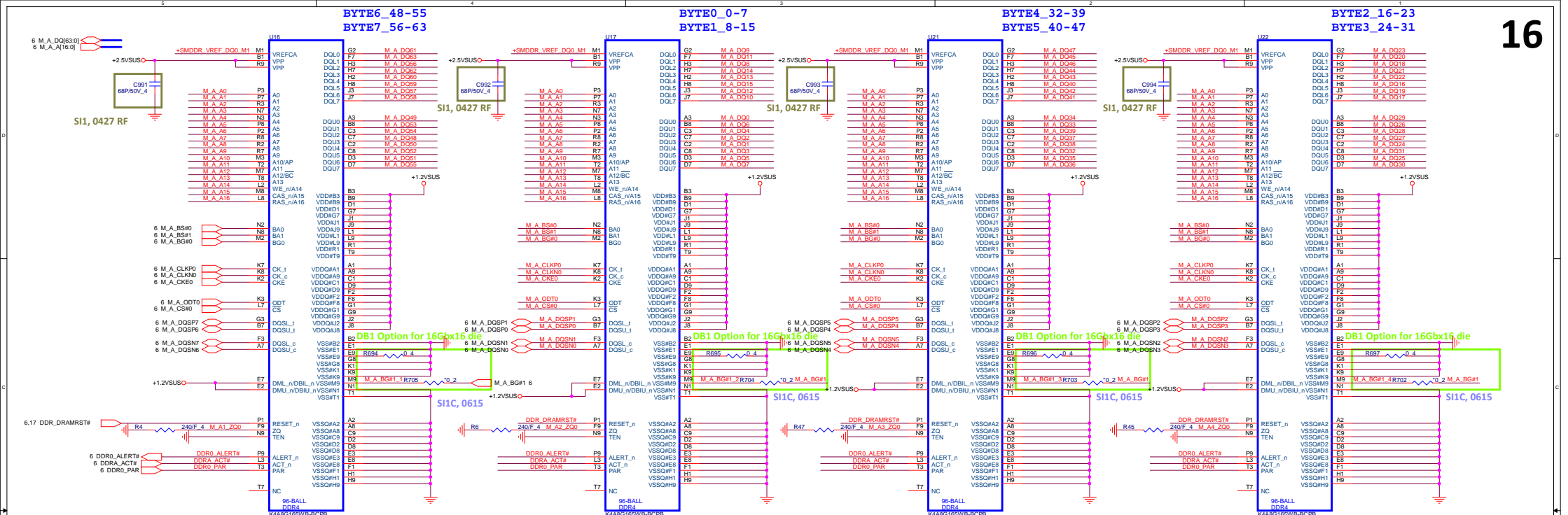
+3VPCU 3,10,18,27,28,30,32,33,35,36,39,41,43,44,45,46,47,48,49,50,51,52,53,54,55,60,61,62,63,64,65,66



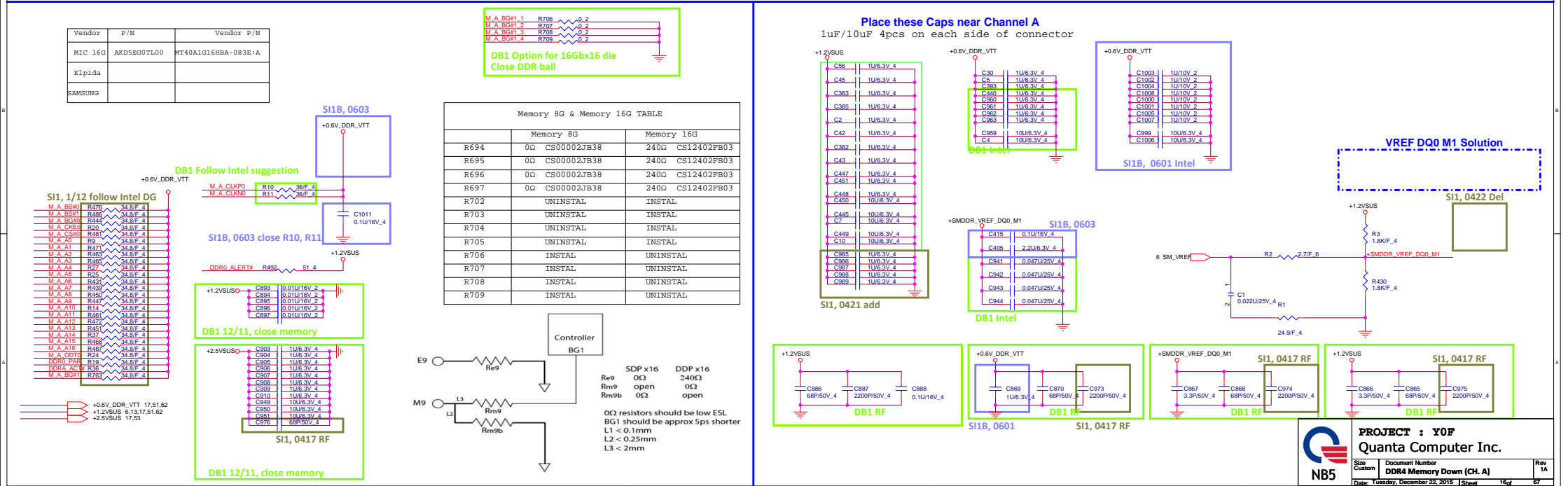
PROJECT : Y0F  
Quanta Computer Inc.

Size	Document Number	Rev
	SKYLAKE XDP & APS	1A
Date: Tuesday, December 22, 2015	Sheet 15 of 67	






Vendor	P/N	Vendor P/N
MIC 16G	AKD5EG0TL00	MT40A1G16HBA-083E:A
Elpida		
SAMSUNG		

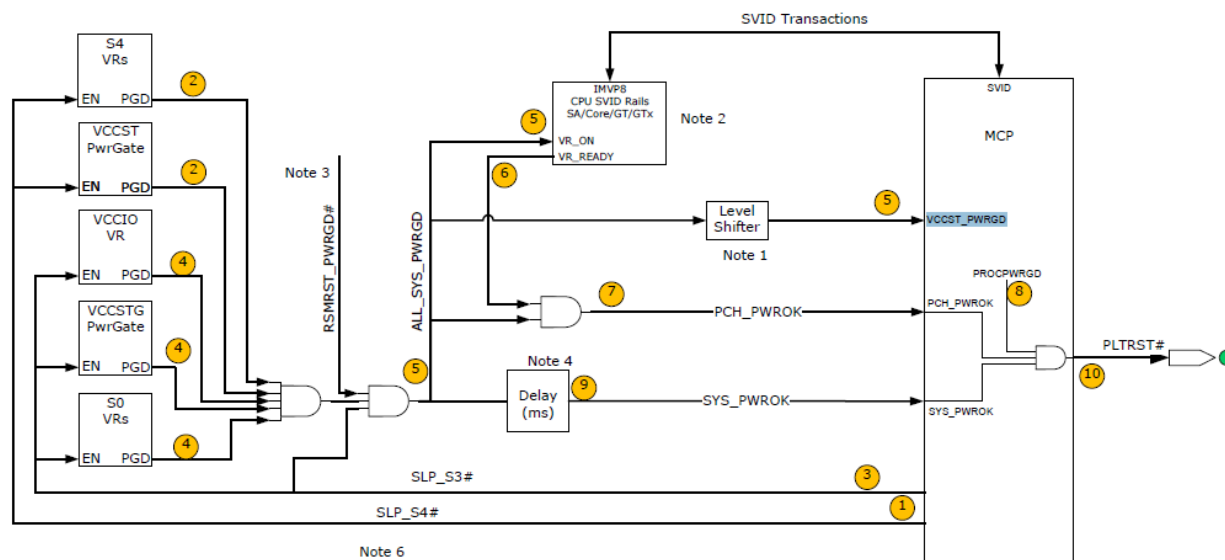
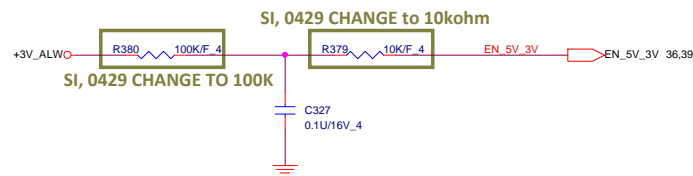
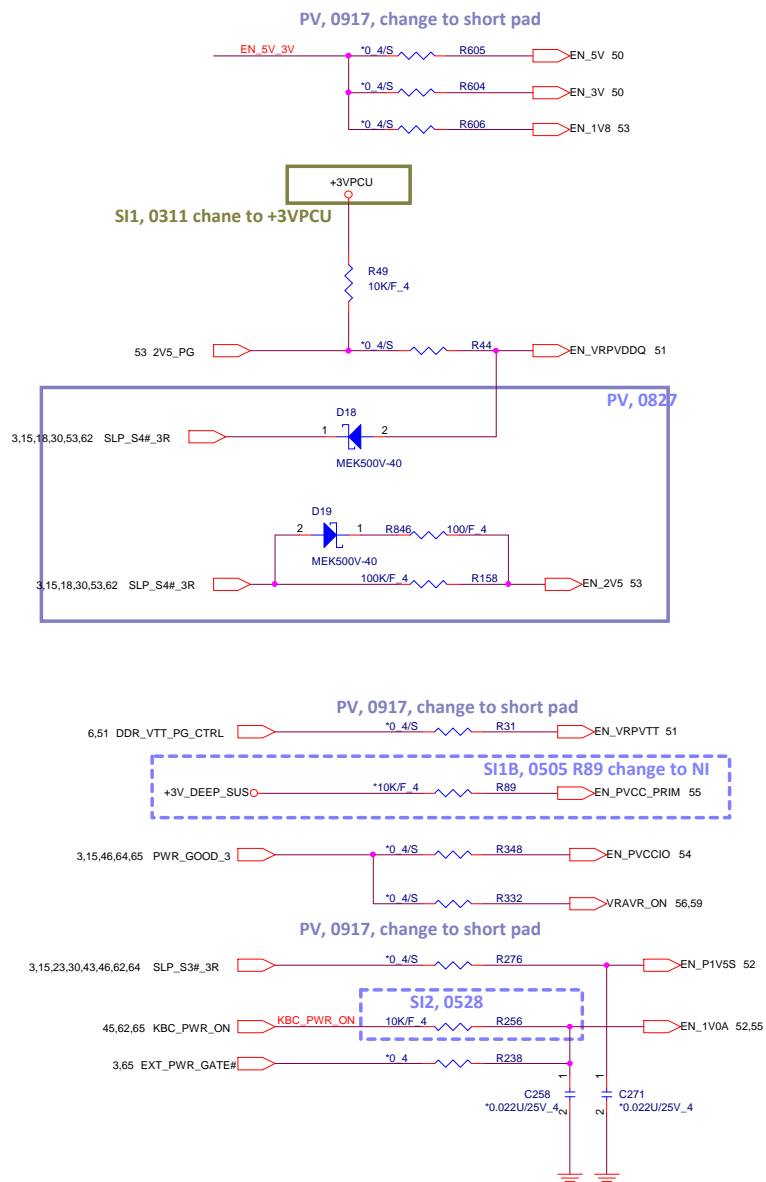


BYTE4\_32-39  
BYTE5\_40-47

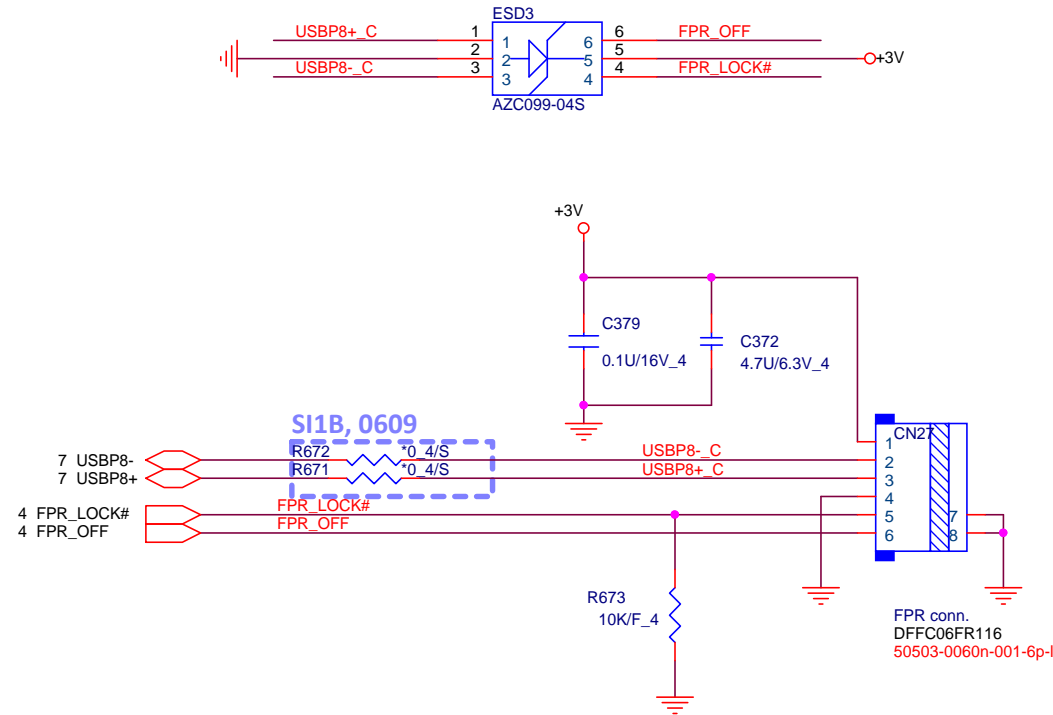
BYTE2\_16-23  
BYTE3\_24-31

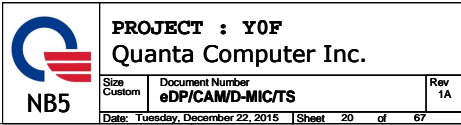


 NB5	<b>PROJECT : Y0F</b> <b>Quanta Computer Inc.</b>		Rev 1A
	Size Custom	Document Number <b>DDR4 Memory Down (CH. B)</b>	
Date: Tuesday, December 22, 2015		Sheet 17 of 67	



# Fingerprint Conn





MODE = L: Control Switching Mode, HDMI ID disable  
= H: Automatic Switching Mode, HDMI ID disable  
= M: Automatic Switching Mode, HDMI ID enable

```
TMDS_DDCBUF = L: DDC pass through
              = H: DDC active buffer
              = M: DDC pass through with 40 kohm pull up resistor
```

```
DP_CFG0 = L: default, automatic EQ enable & AUX interception enable
          = H: automatic EQ disable & AUX interception enable
          = M: automatic EQ disable & AUX interception disable, no pre-emphasis, 800mVpp swing
```

PVR,10/19

- PEQ = L: default, LEQ, compensate channel loss up to 12dB @ HBR2
- = H: HEQ, compensate channel loss up to 15dB @ HBR2
- = M: LLEQ, compensate channel loss up to 5dB @ HBR2

```
TMDS_PRE = L: no pre-emphasis
           = H: 1.5dB pre-emphasis
           = M: 3.0dB pre-emphasis
```

DOCK\_ID1==> HIGH, DP PRIORITY 1  
DOCK\_ID1==> LOW, HDMI PRIORITY 1

SI1, 0424 Add

27  
28 **Need apply PN**

```
DP_CFG1 = L: default, auto test disable & input offset cancellation enable
         = H: auto test enable & input offset cancellation enable
         = M: auto test disable & input offset cancellation disable
```

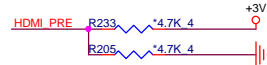
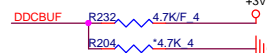
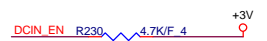
```
TMDS_RT = L: Standard open drain driver
         = H: Open drain driver with termination resistors
```



Size Custom	Document Number <b>DEMUX 8339A</b>	Rev 1A
Date: Tuesday, December 22, 2015		Sheet 21 of 67

3 Level Input:  
L: LOW, internal pull down  
H: HIGH, external pull up  
M: VDD33/2, both external pull-up and pull-down

VCC = 1.2V or 1.35V

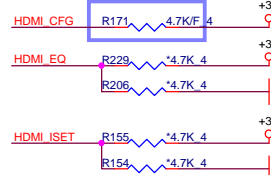


DC coupling enable; Internal pull down at ~150k $\Omega$ , 3.3V I/O.  
L: default, AC coupling input  
H: DC coupling input

Enable active DDC buffer; Internal pull down at ~150K $\Omega$ , 3.3V I/O

- L: default, passive DDC pass-through
- H: active DDC buffer with default threshold
- M: active DDC buffer without internal pull up resistor

```
Output pre-emphasis setting; Internal pull down at ~150k次, 3.3V
I/O.
L: no pre-emphasis
H: 1.6dB pre-emphasis
M: 2.5dB pre-emphasis
```



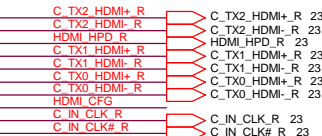
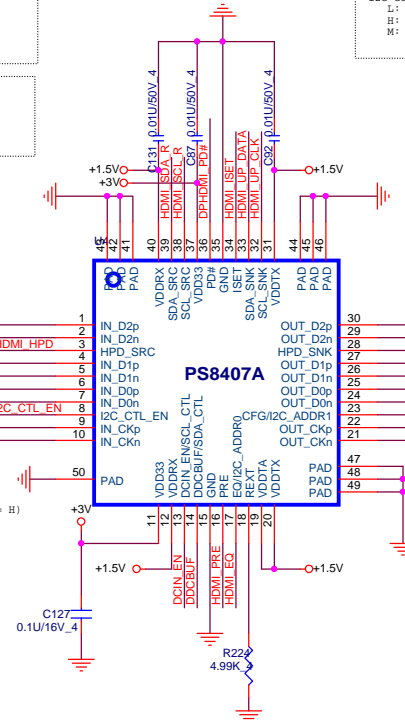
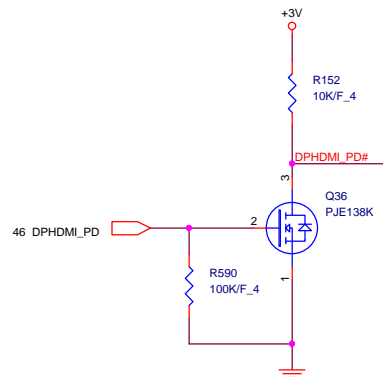
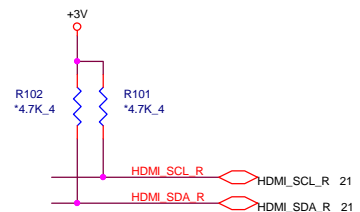
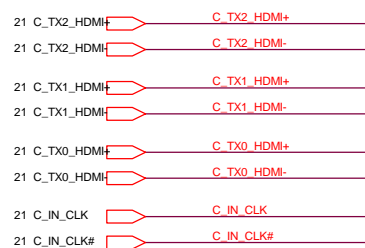
```
Configuration pin, 3.3V IO, internal pull down at ~150k次. 3.3V
I/O.
L: HDMI ID disable
H: HDMI ID enable
```

Receiver equalization setting; Internal pull down at ~150k次, 3.3V I/O.

- L: programmable EQ for channel loss up to 12.4dB
- H: programmable EQ for channel loss up to 4.3dB
- M: programmable EQ for channel loss up to 8.6dB

```
TMDS output swing adjustment; Internal pull down at ~150k $\Omega$ , 3.3V
I/O.
L: default
H: increase +13%
M: reduce -13%
```

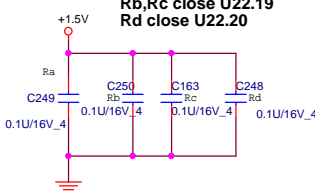
I2C Control enable. Internal pull down at 150k 次 @ 20%. 3.3V I/O.  
 L: Pin Control is selected with auto jitter cleaning (default)  
 H: I2C Control is selected with default I2C address  
 M: Pin control is selected with full jitter cleaning



### HDMI Source Receptacle Connector

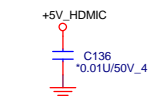
## PS8407A Pin Control Mode

Ra close U22.12  
Rb,Rc close U22.19  
Rd close U22.20



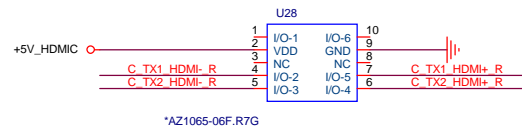


22 HDMI\_UP\_DATA HDMI\_UP\_DATA  
22 HDMI\_UP\_CLK HDMI\_UP\_CLK

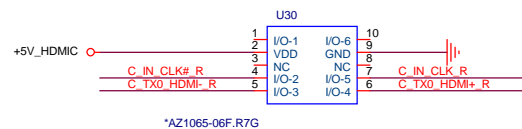


for EMI request

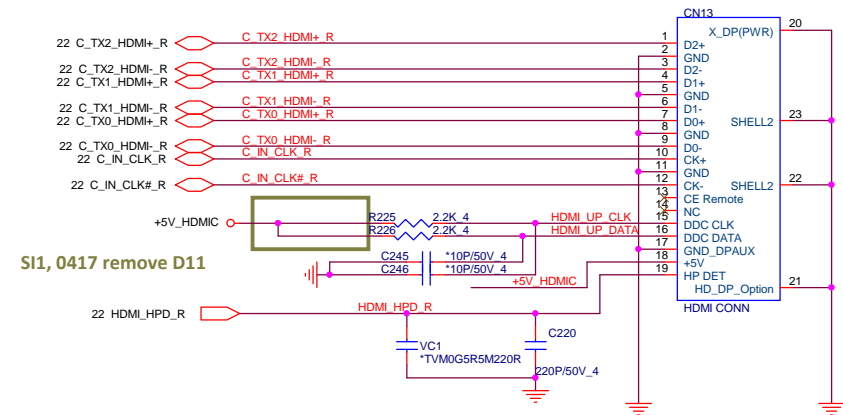
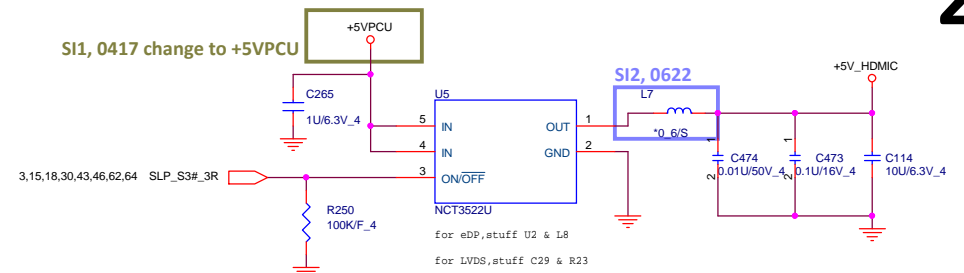
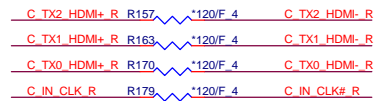
ESD chip, reserve



ESD chip, reserve



### EMI Solution

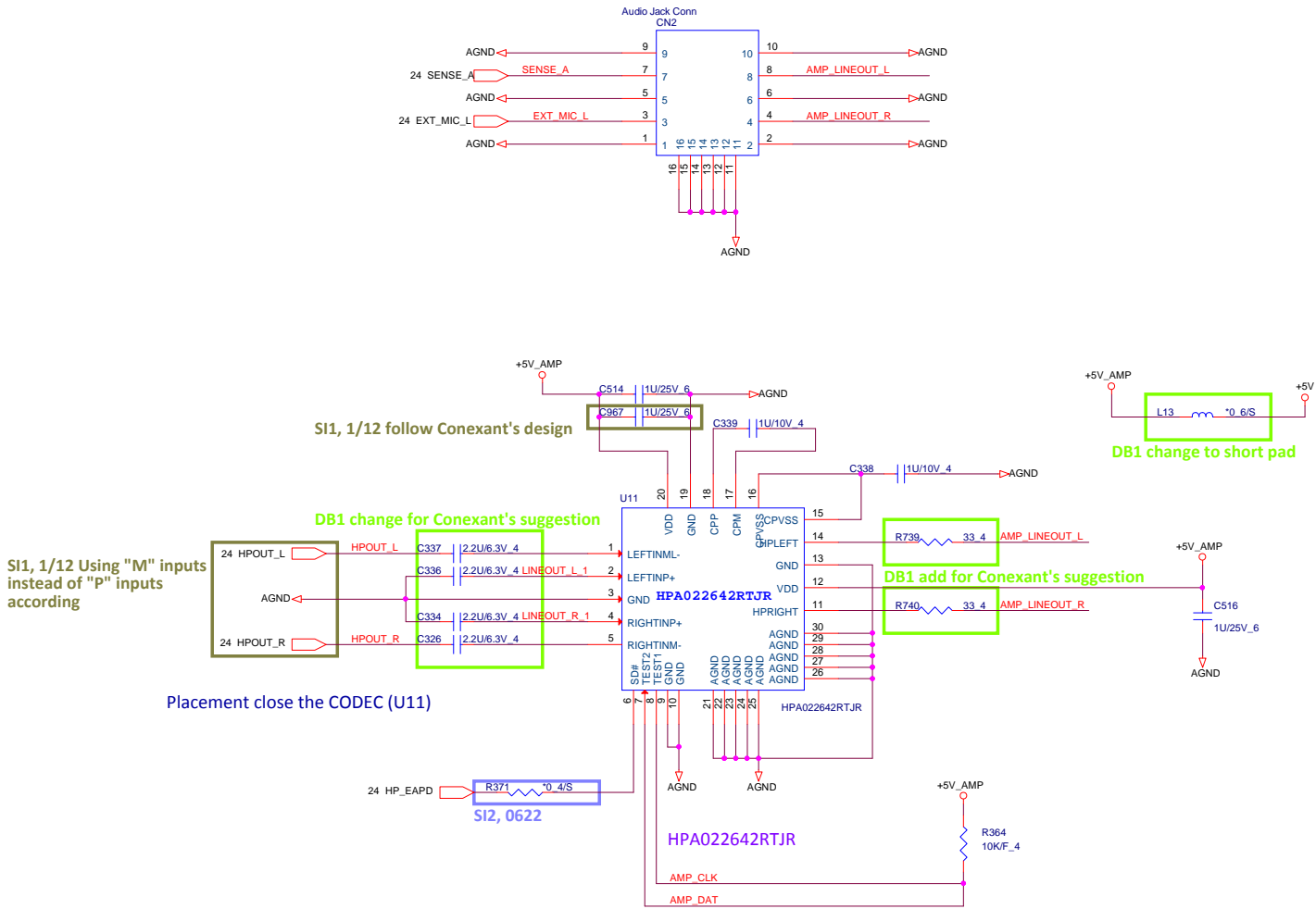


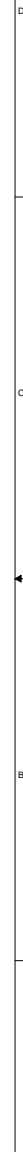
PROJECT : Y0F  
Quanta Computer Inc.

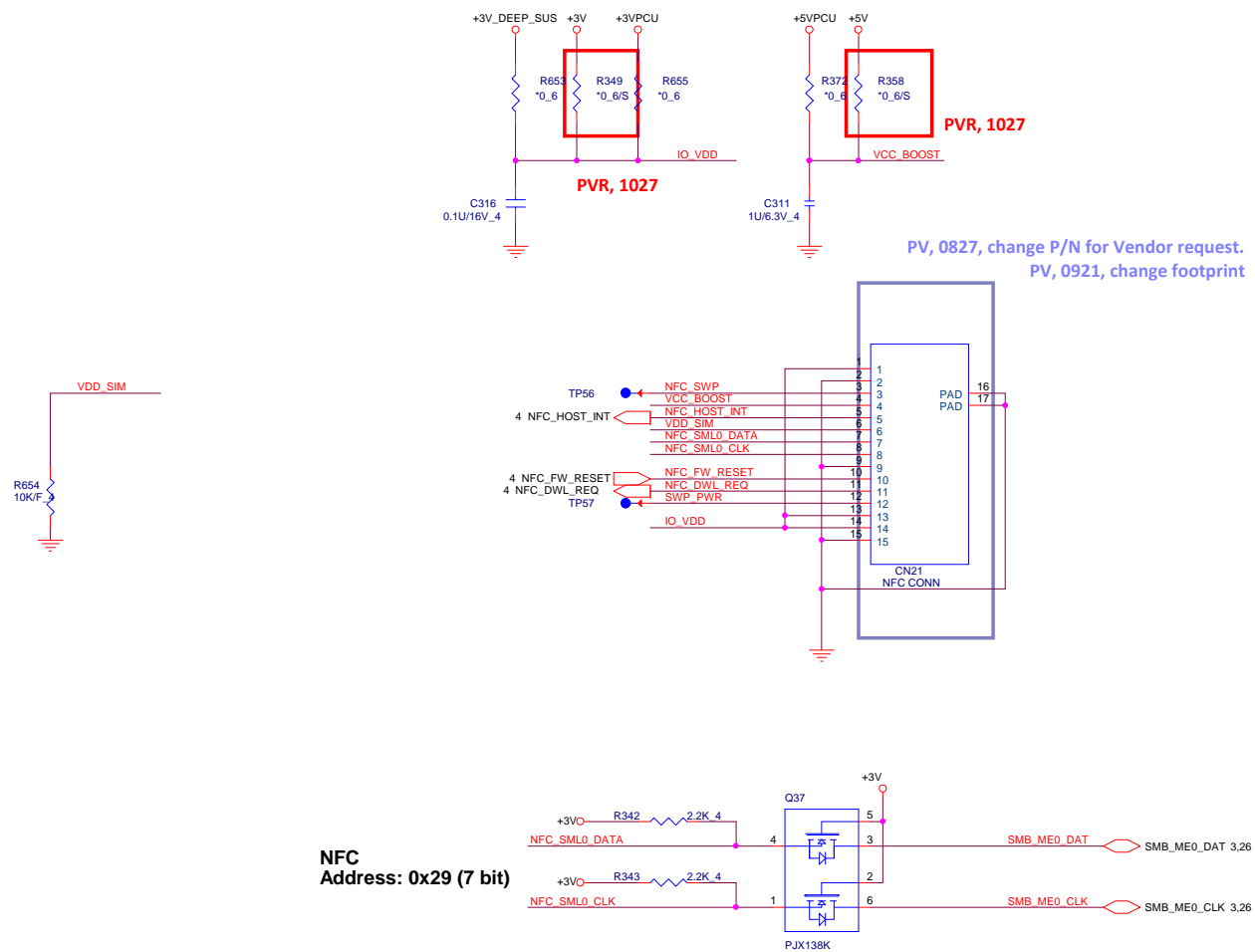
Size Custom	Document Number HDMI CONNECTOR	Rev 1A
Date: Tuesday, December 22, 2015	Sheet 23 of 67	



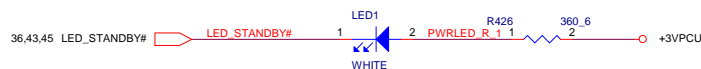
Head Phone/MIC combo jack/AMP



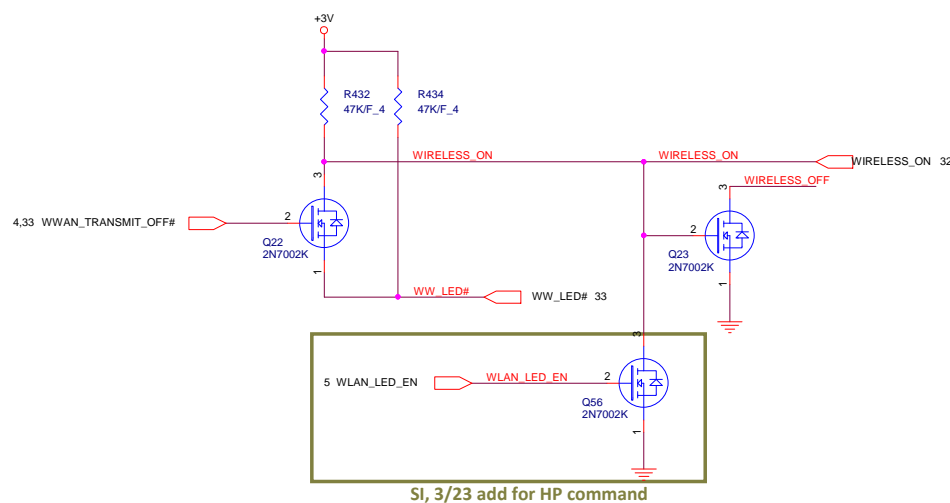
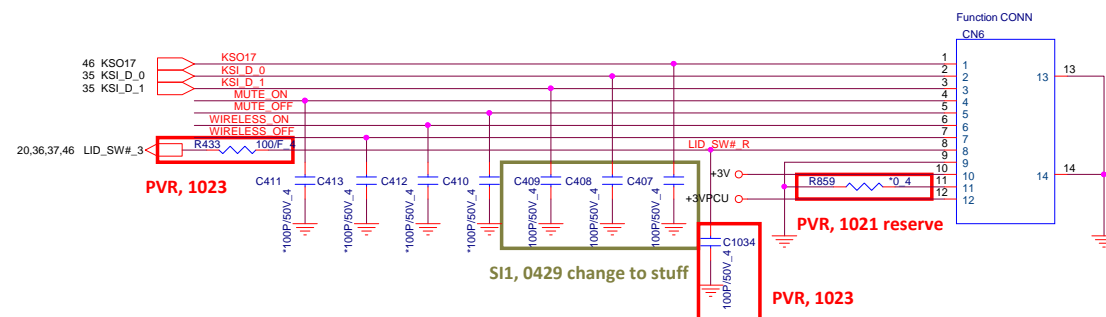
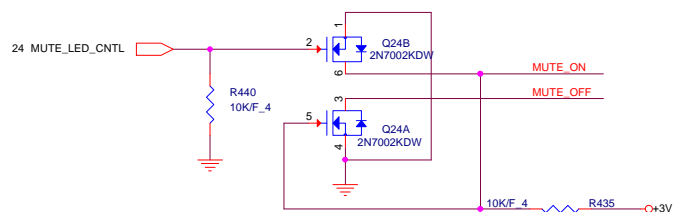
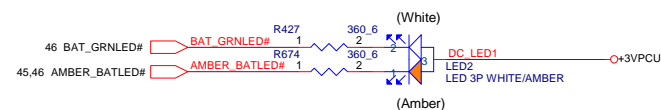





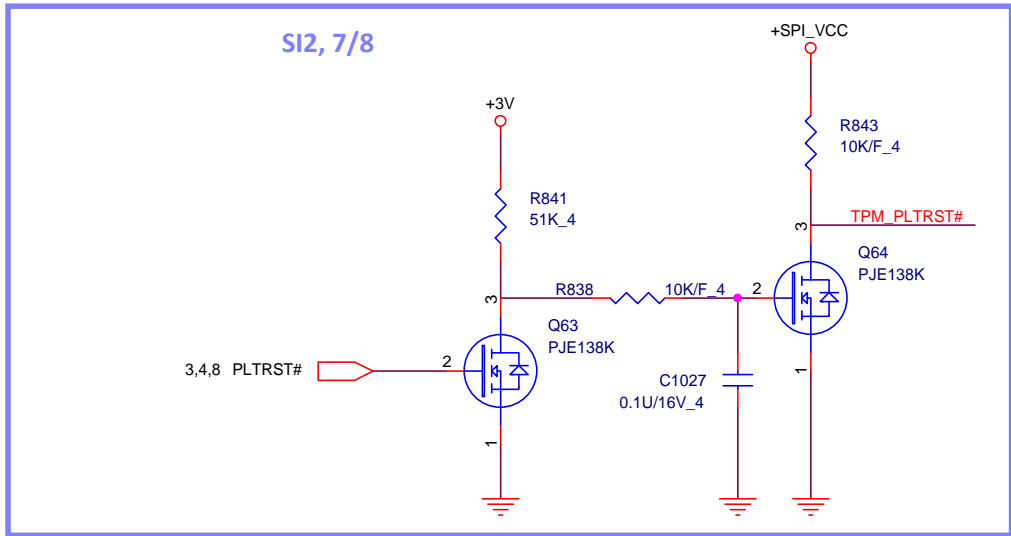
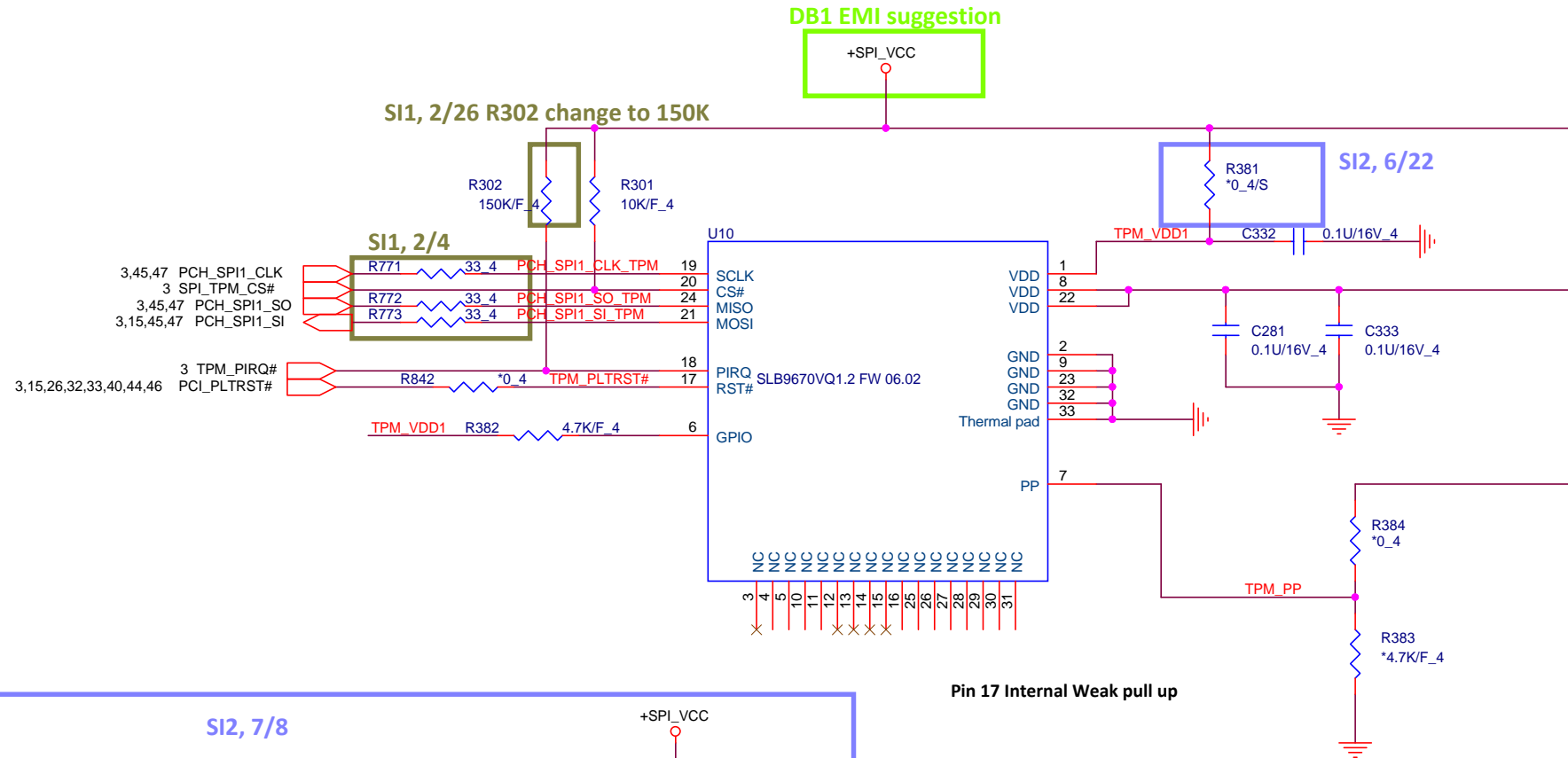
## PWR LED



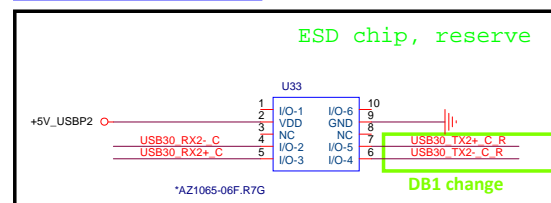
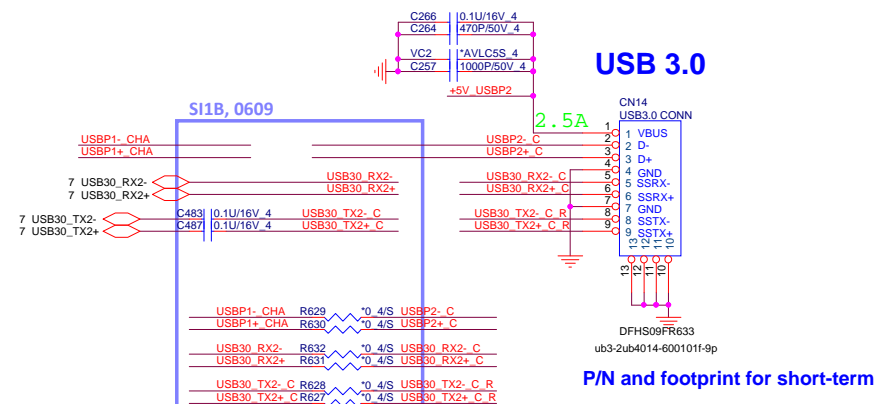
## Battery LED



 NB5	PROJECT : Y0F		
	Quanta Computer Inc.		
	Size	Document Number	Rev
	Custom	LED & Function Conn.	1A
Date: Tuesday, December 22, 2015   Sheet 28 of 67			

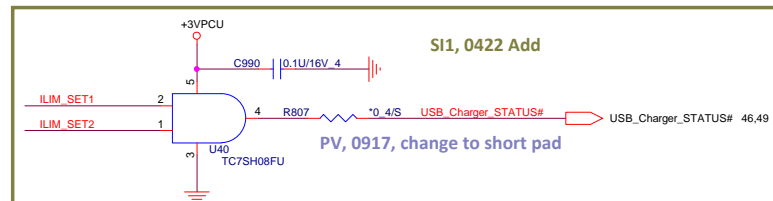
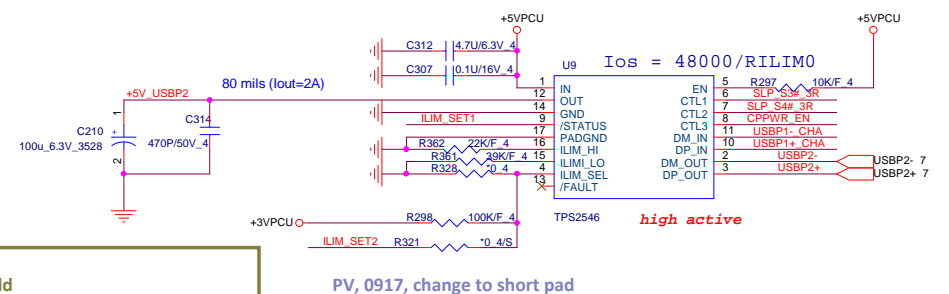


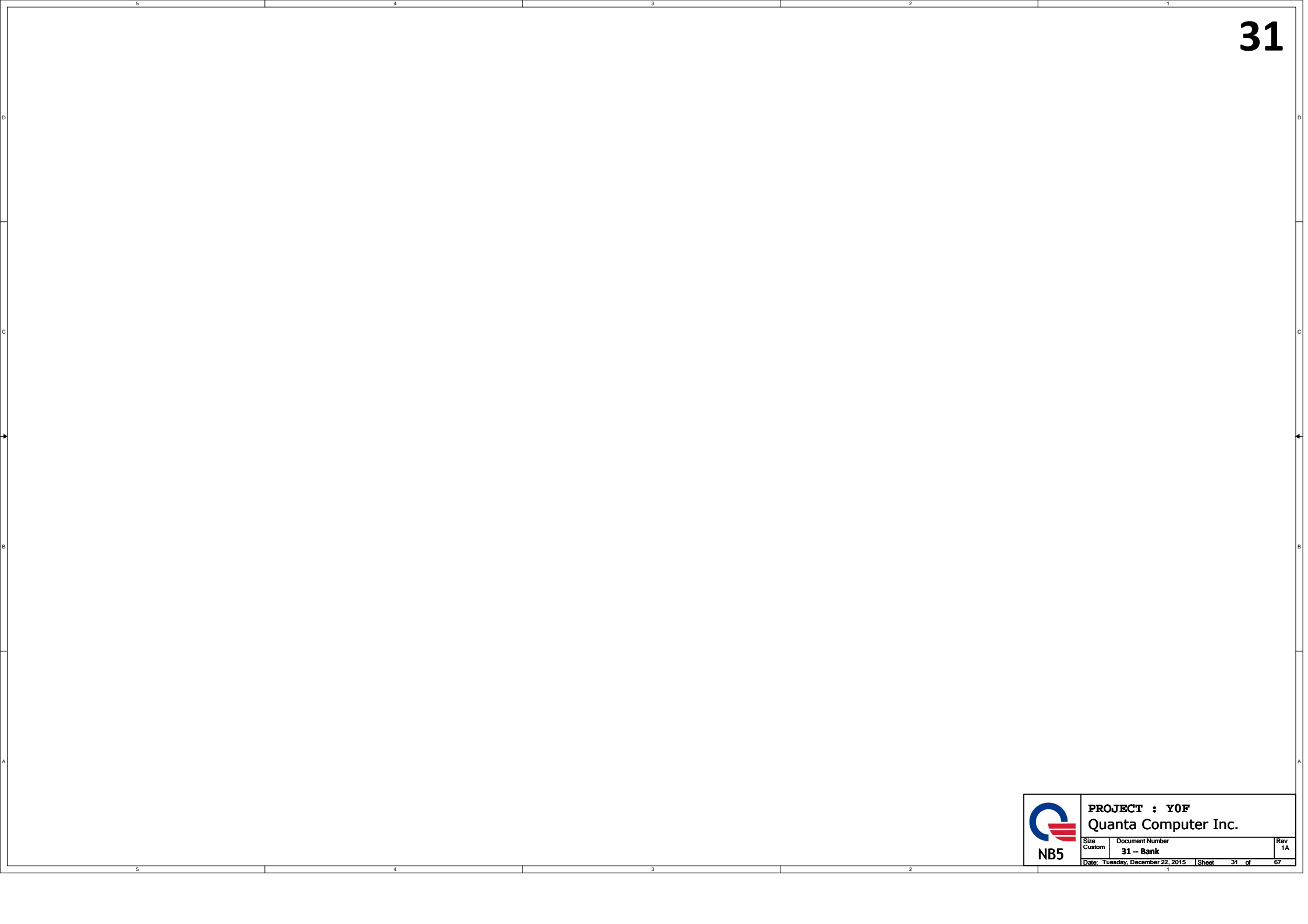





## USB Charger

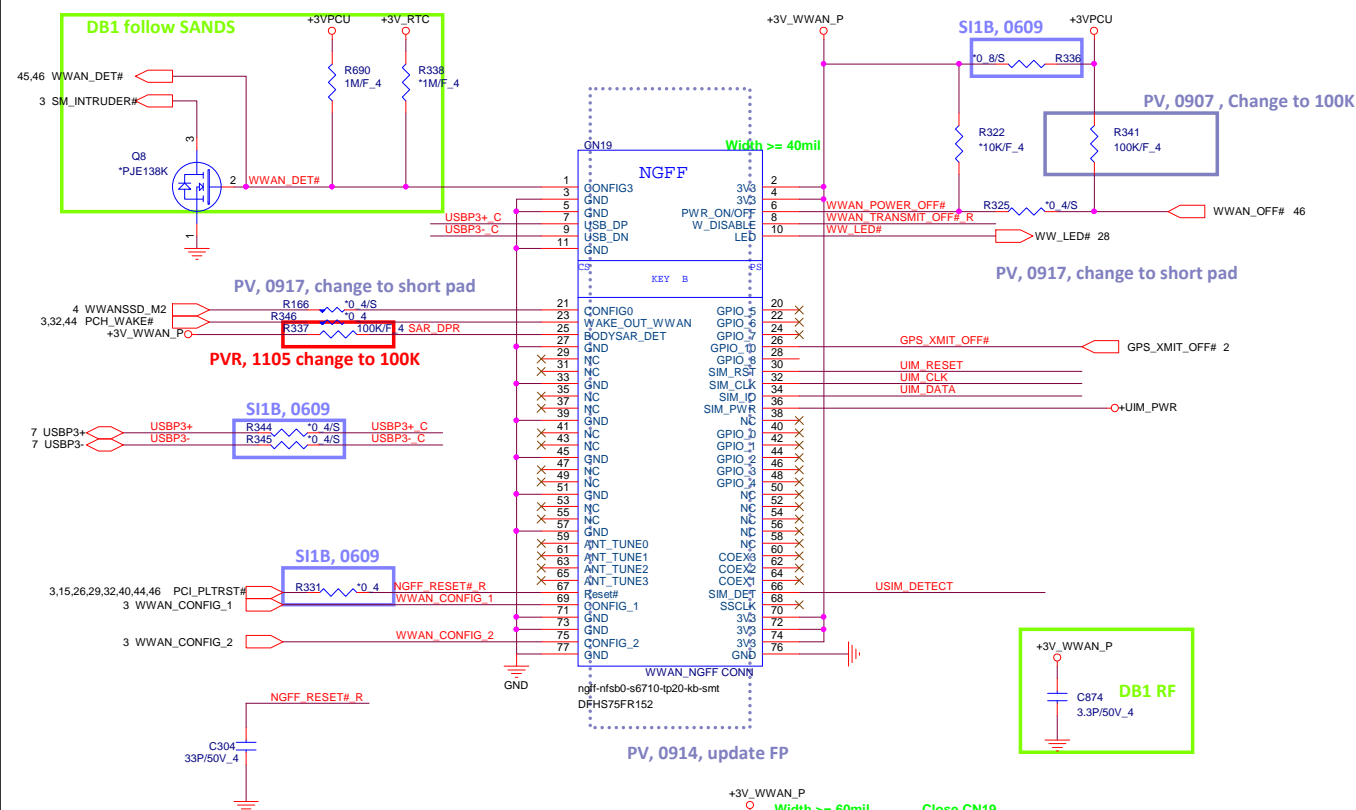
IC continuous output current is 2.5A



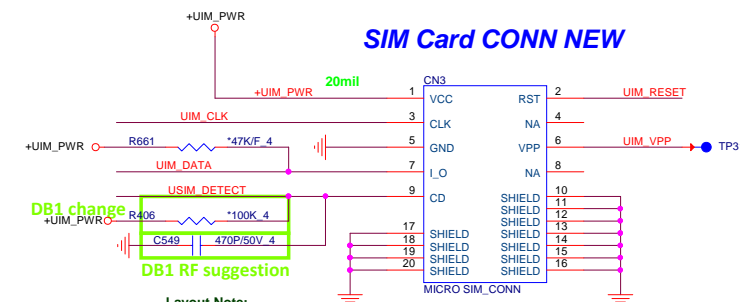


 NB5	<b>PROJECT : Y0F</b> <b>Quanta Computer Inc.</b>		
	Size Custom	Document Number <b>31 -- Bank</b>	Rev 1A
	Date: Tuesday, December 22, 2015   Sheet 31 of 67		



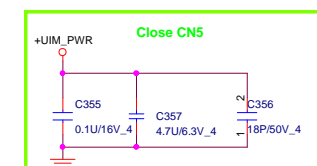
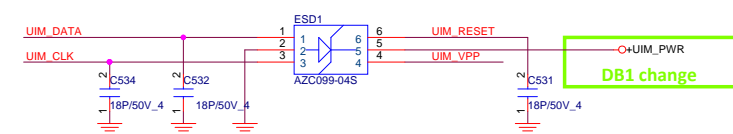


**SIM Card CONN NEW**



**Layout Note:**

1. UIM\_RESET, UIM\_CLK, UIM\_DATA routing as short as possible  
Route into ESD then go out
2. Avoid routing the SIM\_CLK and SIM\_DATA lines in parallel over distances  $\geq 2$  cm
3. Position the SIM connector from the WWAN module  $\leq 100$ mm if possible,  
NOT exceed length is 150mm.



## Trace Length and Routing

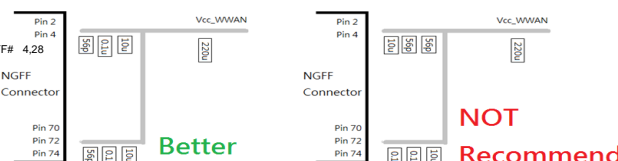
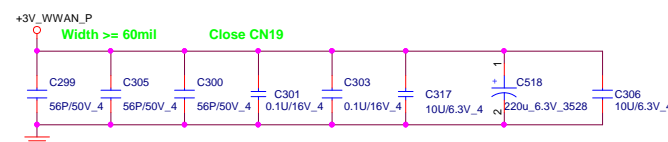
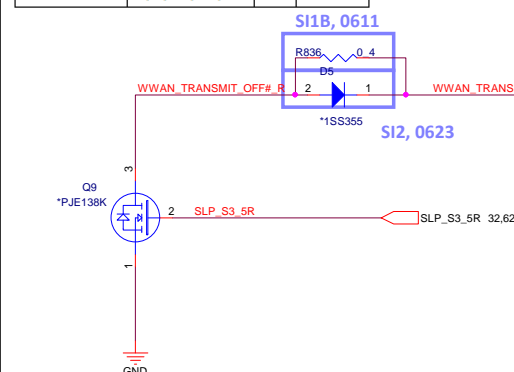
- Special attention should be paid to SIM traces (UIM\_CLK, UIM\_DATA and UIM\_RST) to minimize the trace lengths between the SIM slot and the WAN NGFF slot. **Minimizing the signal lengths and traces will reduce possibility of SIM signal integrity issues.** Recommended maximum length is 100mm. Not to exceed length is 150mm.↵
- Minimum distance between UIM\_CLK and UIM\_DATA should be 20 mils. Static signals such as UIM\_RST can be routed between UIM\_CLK and UIM\_DATA to conserve space if needed.↵
- It is recommended that SIM traces be isolated from other high-speed switching signals, as noise can couple into the SIM signals. Keep a minimum distance of 20 mils between UIM\_CLK, UIM\_DATA and any other high-speed switching signals.↵
- Placing the SIM card on a daughter card is also not recommended as the interconnect may impact SIM signal integrity.

## SIM Power4

- The UIM\_PWR trace width must be at least 20 mils. Sub-planar routing is recommended.<sup>4</sup>
- Implement additional power filtering to SIM card power to ensure clean power is supplied to minimize any possible noise ripple effects. At a minimum, place a 0.1uF and a 4.7uF capacitor on the UIM\_PWR supply and locate near the SIM connector.<sup>4</sup>



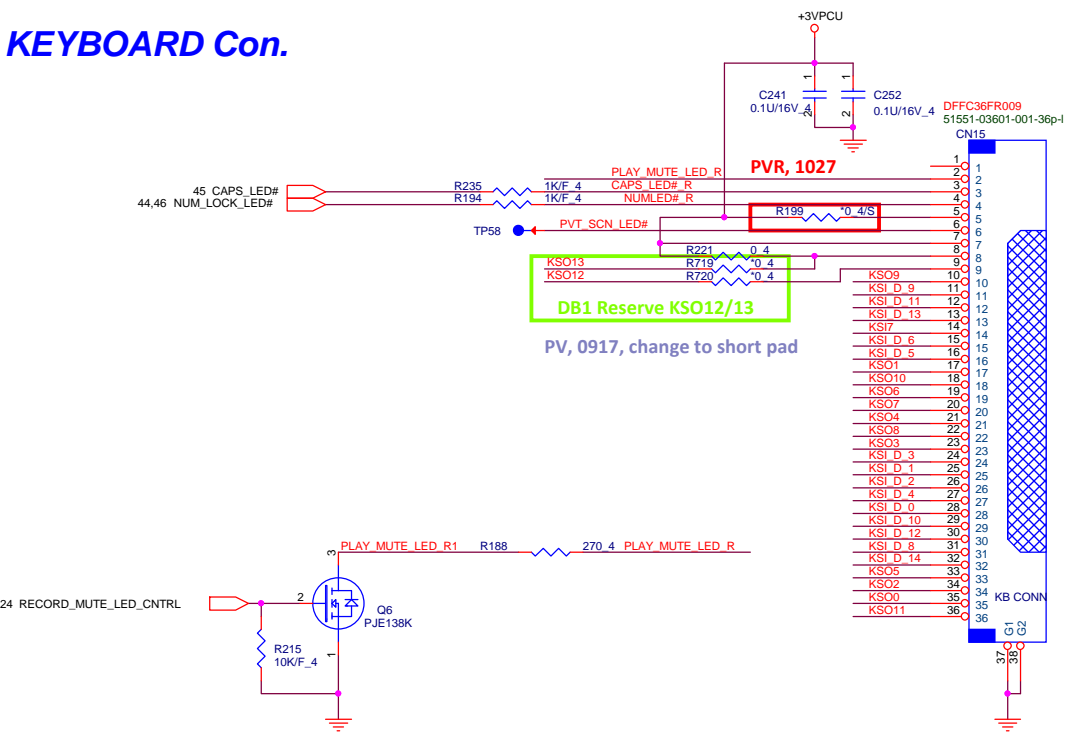
↕	<b>M.2 Pinout</b> ↕	<b>S0</b> ↕	<b>S3 – S5</b> ↕
WWAN 3.3V↕	2, 4, 70, 72, 74↕	On↕	Off ↕



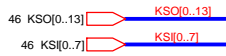
+VCC	Power_On/Off (Pin6)	W_Disable (Pin8)	GPS_Disable (Pin26)
S0 ON	High	High	High
S3 ON	High	Low	Low
S4 ON	Low	Low	Low
S5 ON	Low	Low	Low



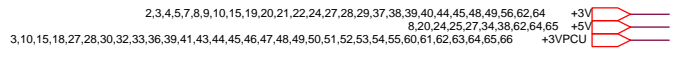
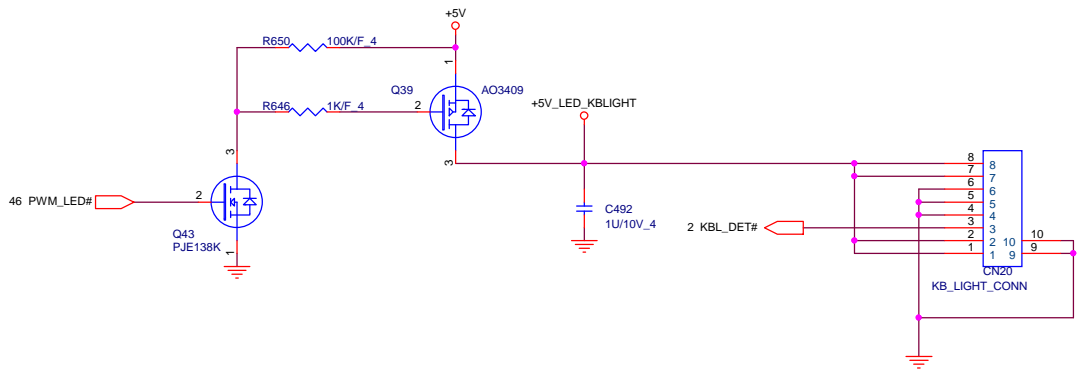
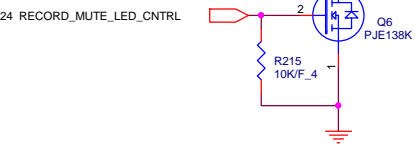
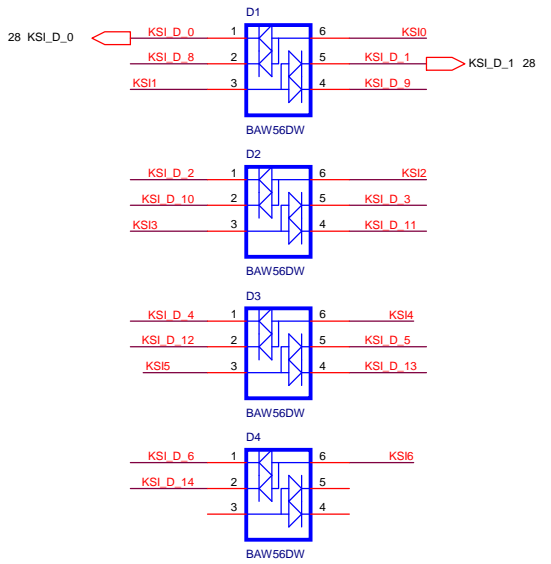
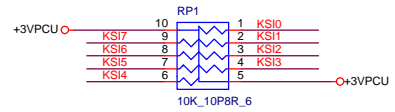
KEYBOARD Con.

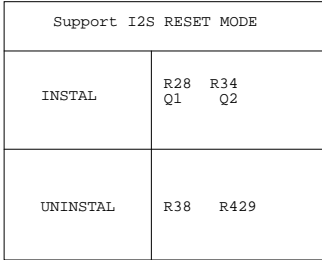


	Olympia	New
R199	Unstuff	Stuff
R221	Stuff	Unstuff



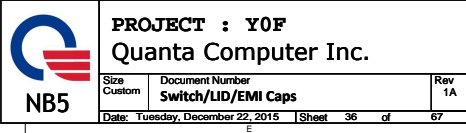
KEYBOARD PULL-UP



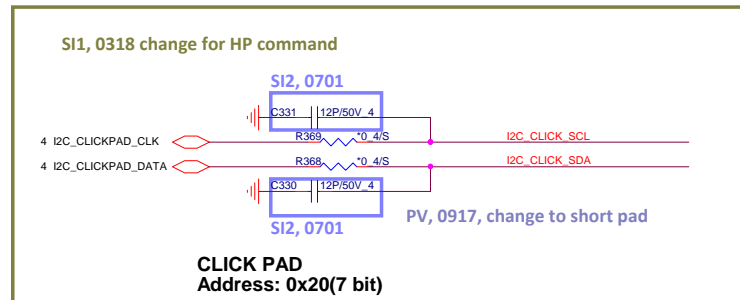
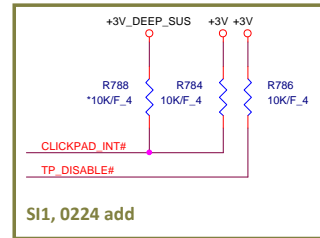
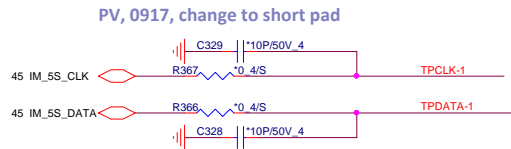


The FT8010 reset timer uses an internal oscillator and a two-stage, 21-bit counter to determine when the output pins switch. Time N is set by the hard-wired logic level of the DSR pin. N is either  $7.5 \pm 20\%$  seconds for DSR=LOW or  $11.25 \pm 20\%$  seconds for DSR=HIGH.

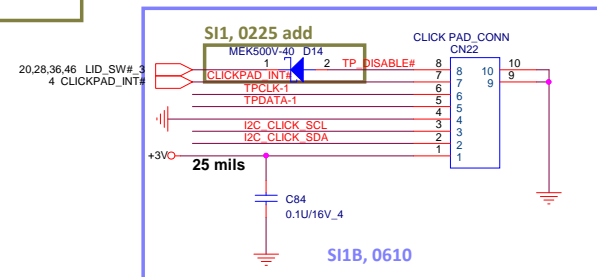
DSR	Reset Timer ( +20% )
0	7.50s
1	11.25s







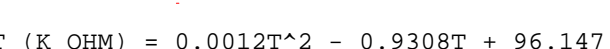
### Click Pad Connector



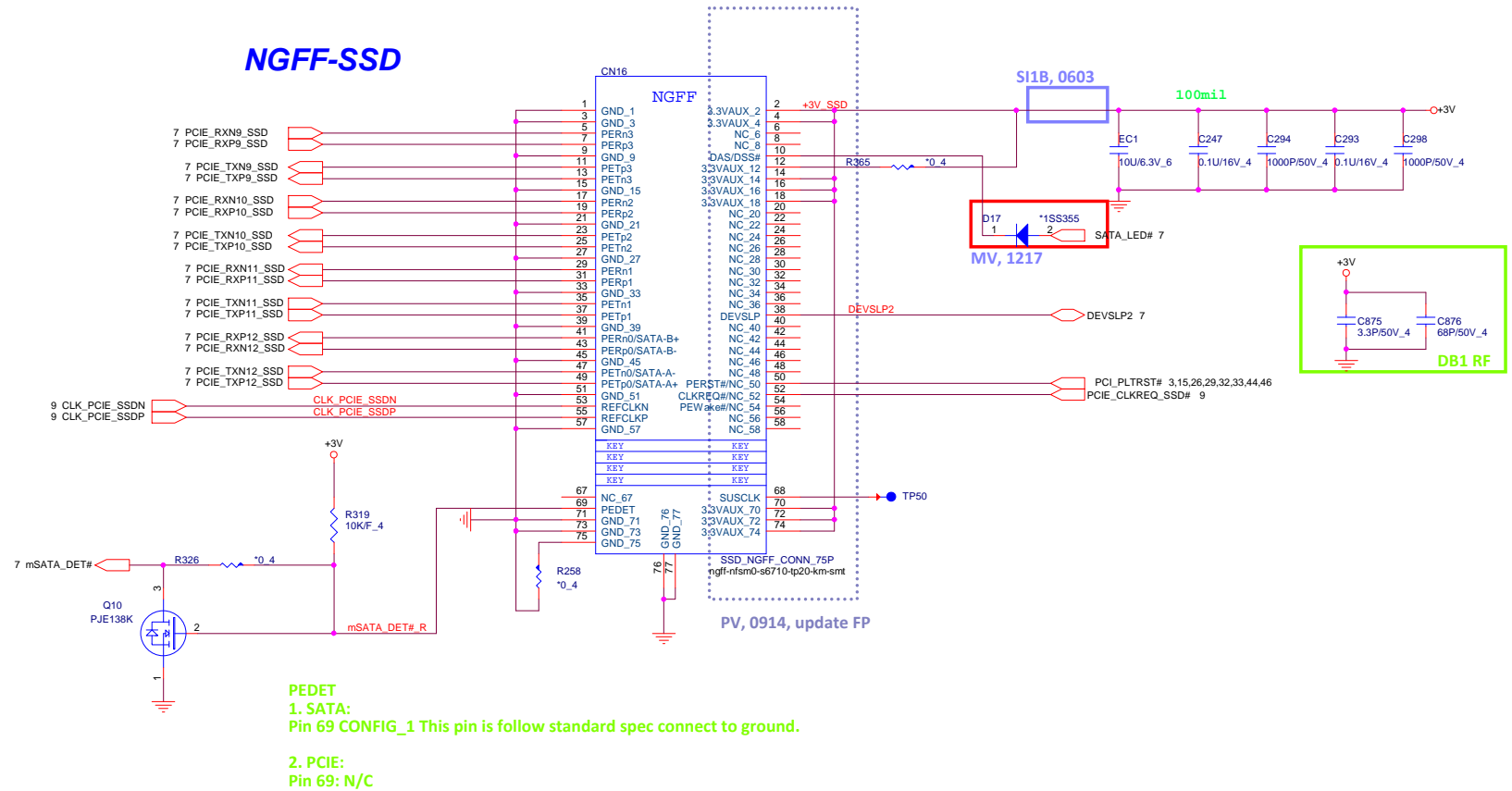
2,3,4,5,7,8,9,10,15,19,20,21,22,24,27,28,29,38,39,40,44,45,48,49,56,62,64  
4,5,8,24,64,65 +1.8V



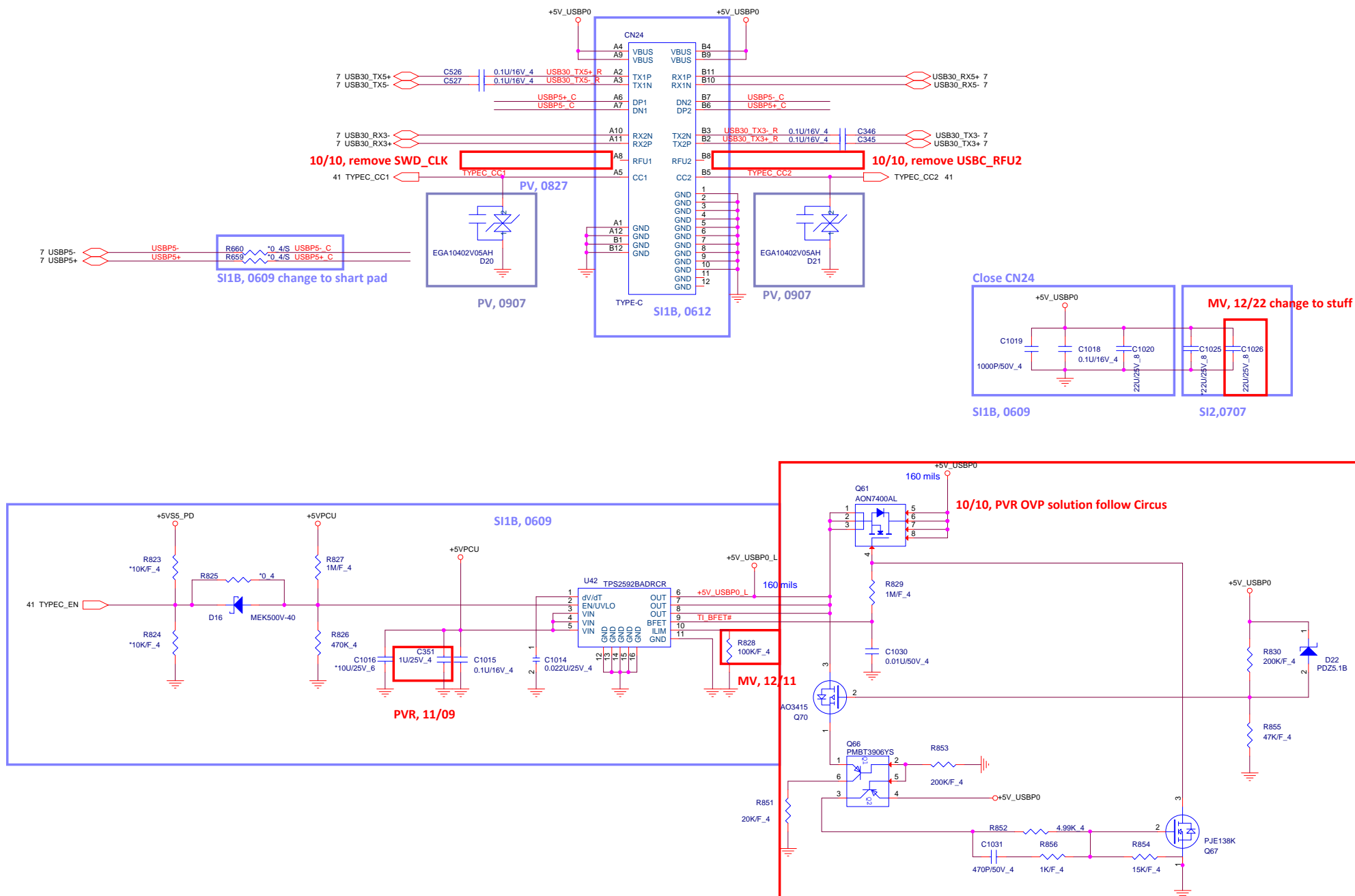
---



--	--

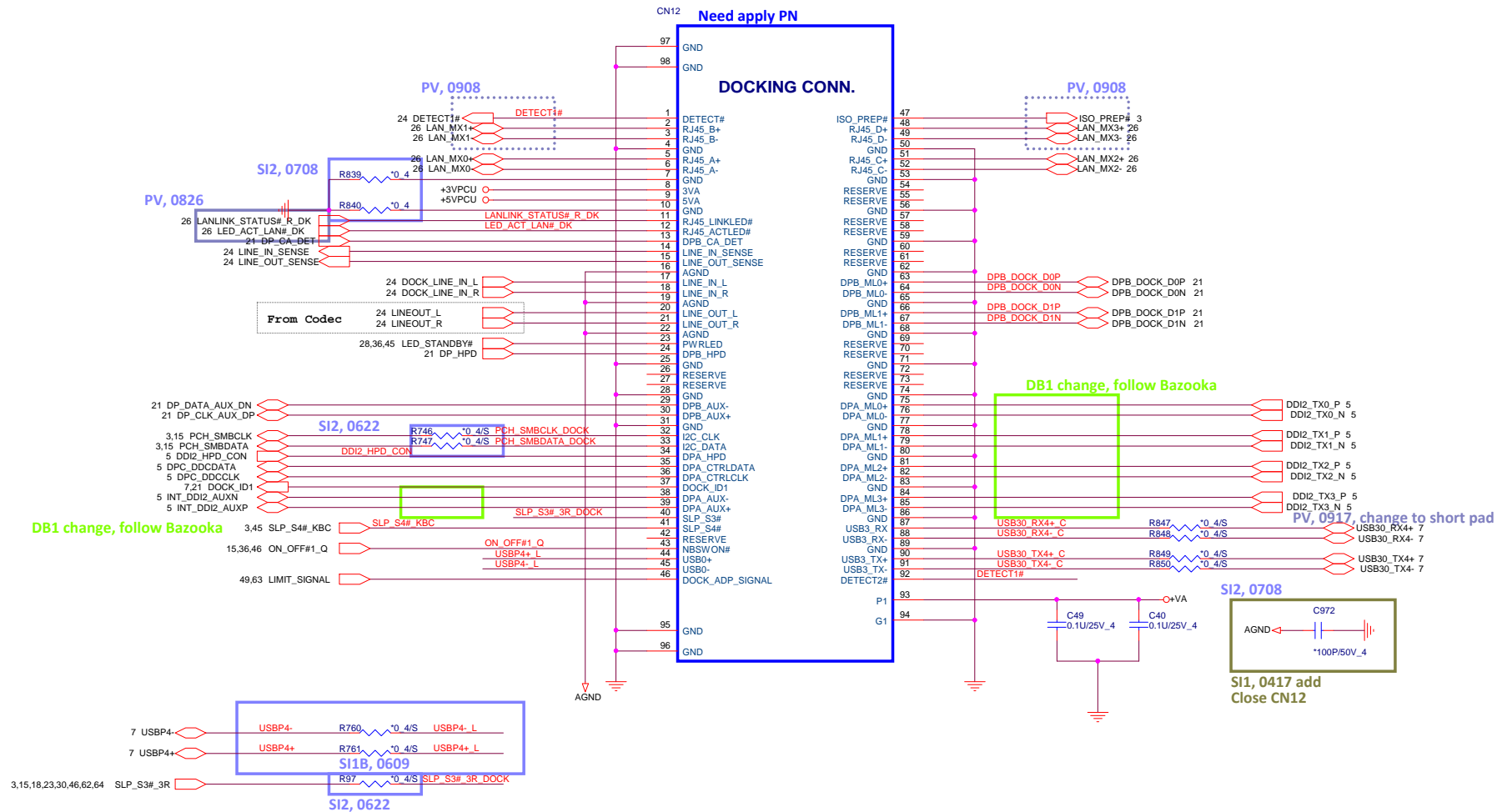




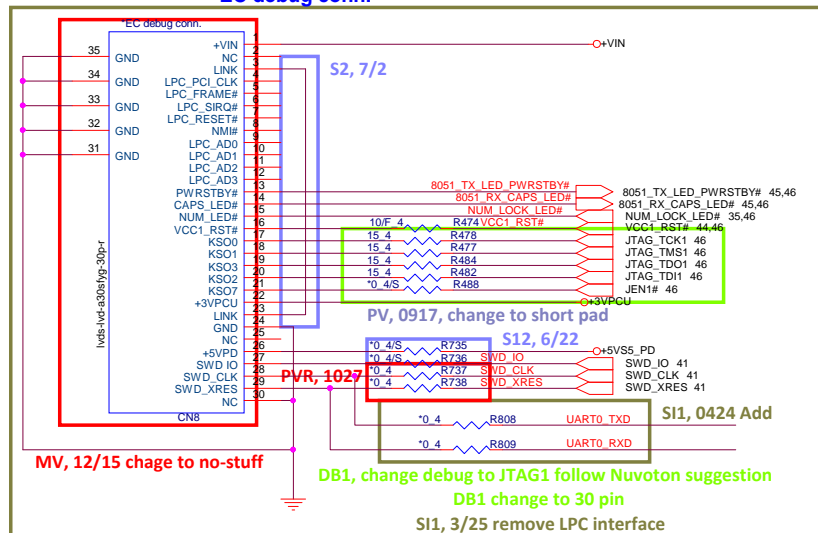


PROJECT : Y0F  
Quanta Computer Inc.

Size	Document Number	Rev
	TYPE-C	1A
Date: Tuesday, December 22, 2015   Sheet 42 of 67		



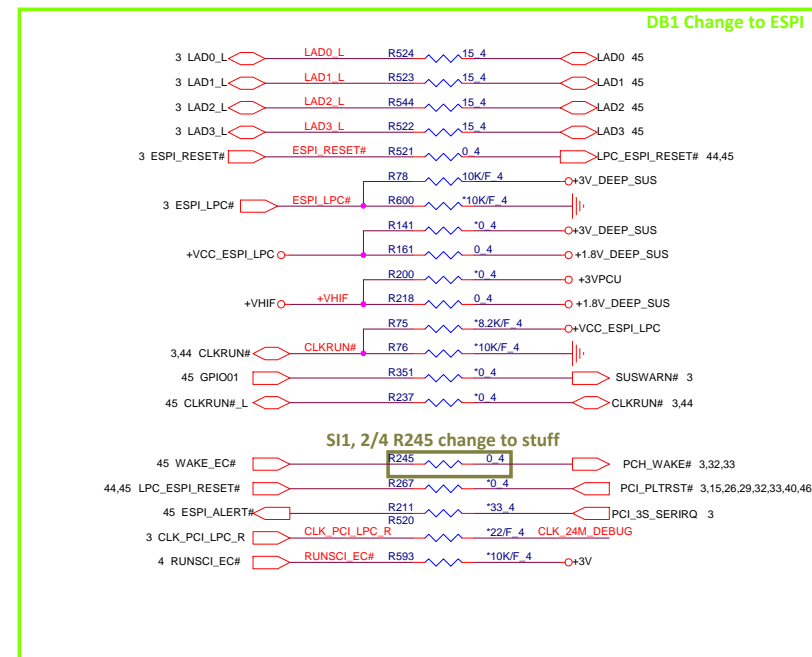
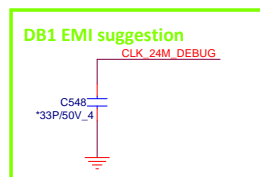
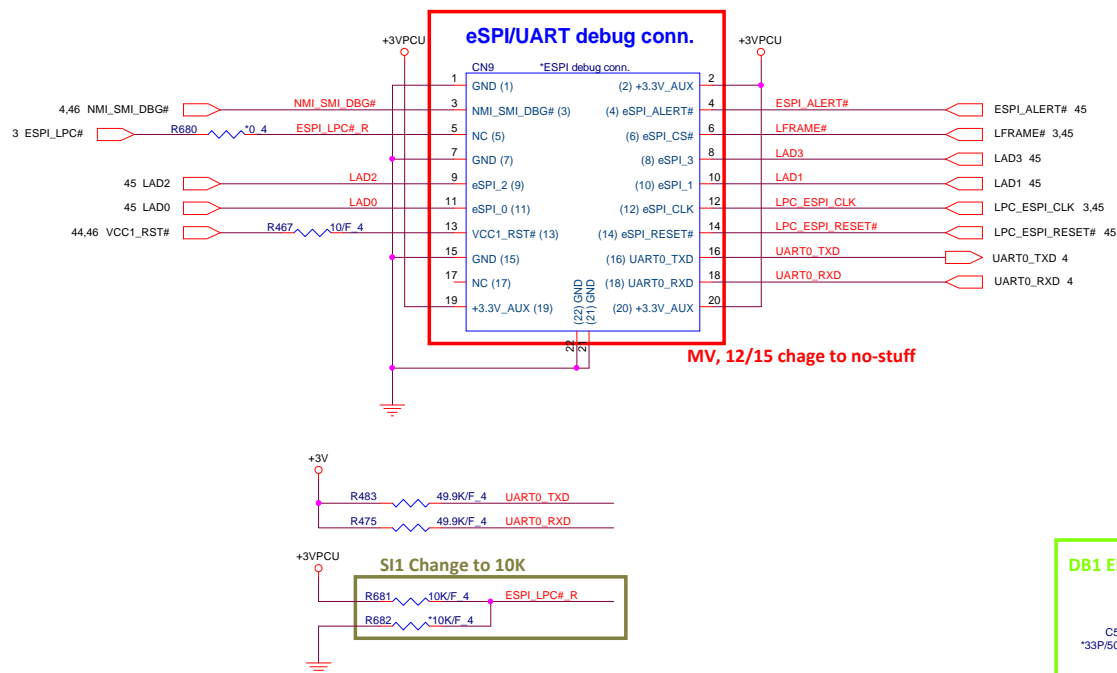
EC debug conn.



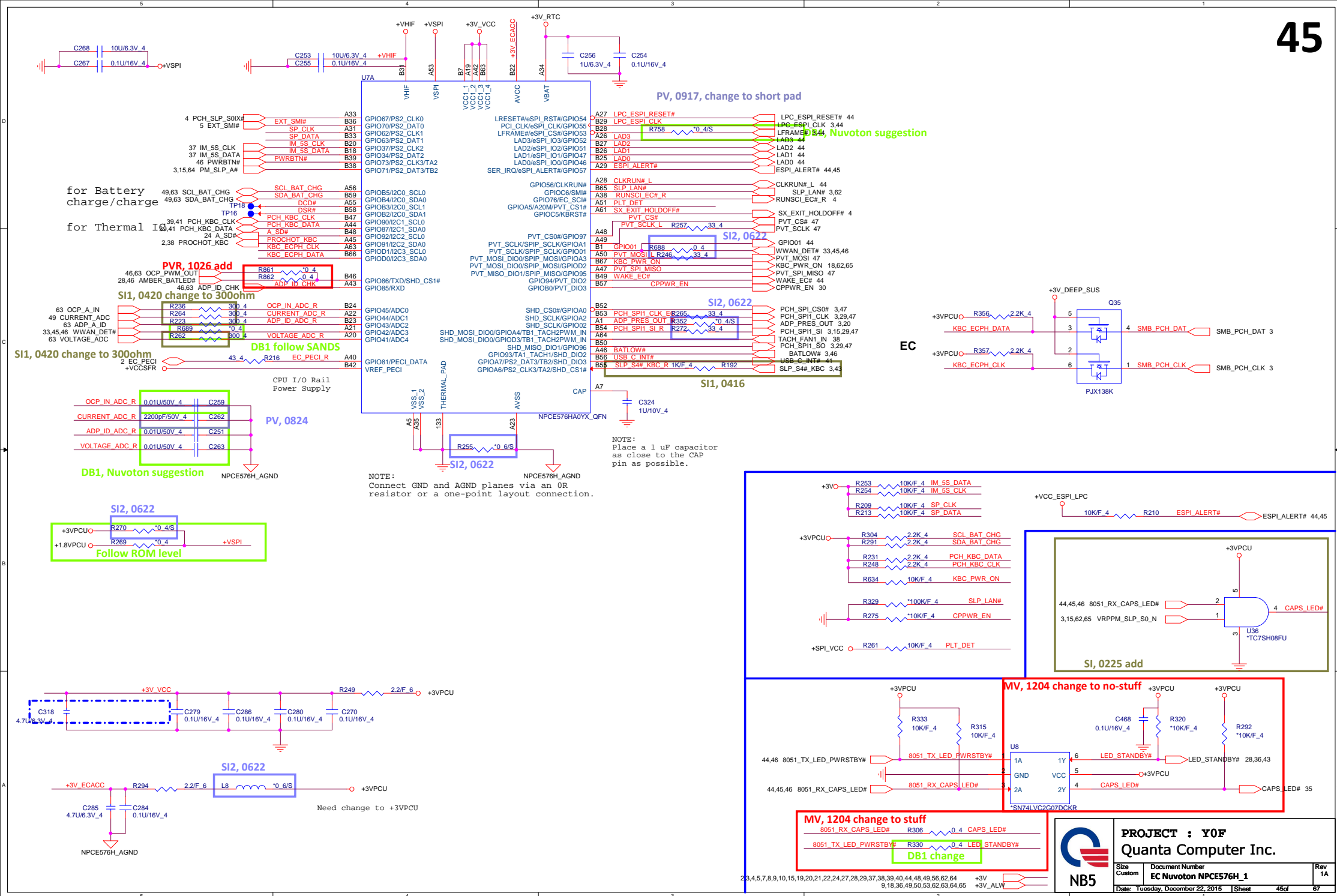
LPC & ESPI TABLE		
	LPC MODE	ESPI MODE
R448	INSTAL	UNINSTAL
R452	INSTAL	UNINSTAL
R457	INSTAL	UNINSTAL
R462	INSTAL	UNINSTAL
R464	INSTAL	UNINSTAL
R470	INSTAL	UNINSTAL

LPC & ESPI TABLE		
	LPC MODE	ESPI MODE
R524	0Ω	15Ω
R523	0Ω	15Ω
R544	0Ω	15Ω
R522	0Ω	15Ω
R521	UNINSTAL	INSTAL
R78	UNINSTAL	INSTAL
R600	INSTAL	UNINSTAL
R141	INSTAL	UNINSTAL
R161	UNINSTAL	INSTAL
R351	INSTAL	UNINSTAL
R237	INSTAL	UNINSTAL
R245	INSTAL	UNINSTAL
R267	INSTAL	UNINSTAL
R211	INSTAL	UNINSTAL
R218	UNINSTAL	INSTAL
R200	INSTAL	UNINSTAL
R75	INSTAL	UNINSTAL
R110	INSTAL	UNINSTAL
R520	22Ω	UNINSTAL
R174	INSTAL	UNINSTAL
R595	INSTAL	UNINSTAL
R592	INSTAL	UNINSTAL
R593		UNINSTAL

LPC & ESPI TABLE		
	LPC MODE	ESPI MODE
R680	INSTAL	UNINSTAL
R681	UNINSTAL	INSTAL
R682	INSTAL	UNINSTAL



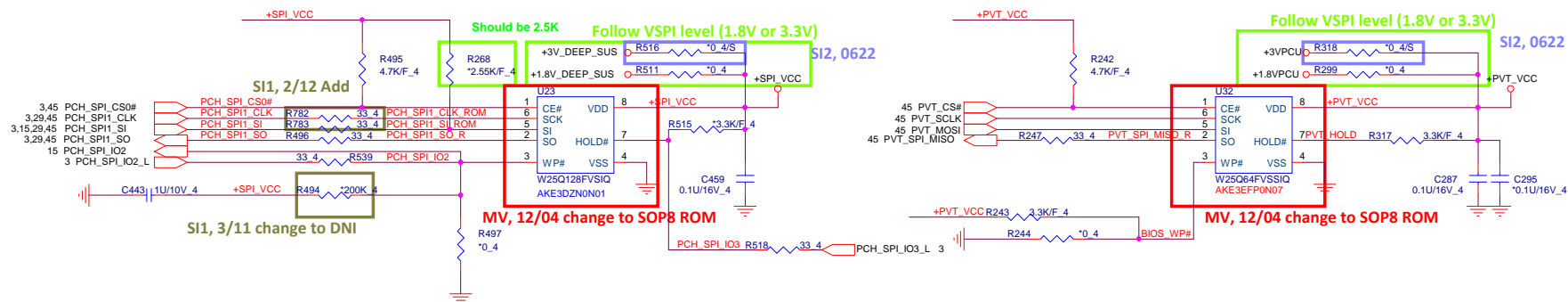




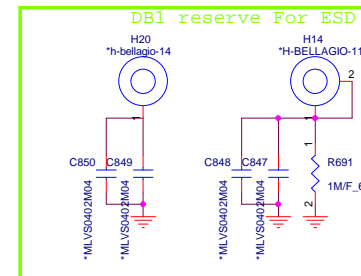
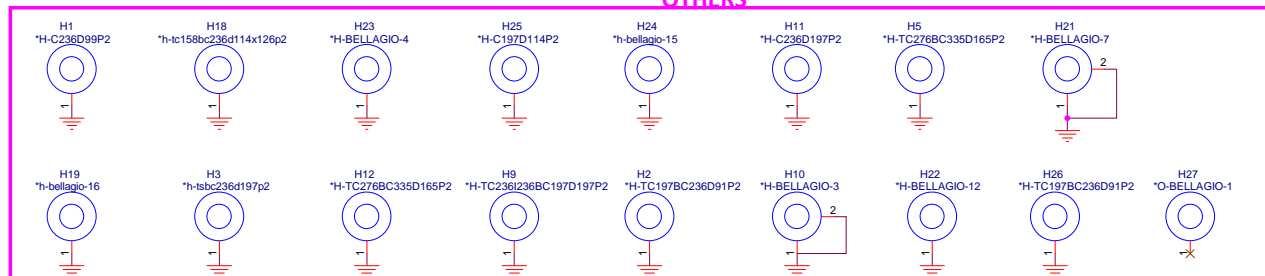


Size	WSN Main(Winbond)	WSN 2nd (GD)	SOP8 Main(Winbond)	SOP8 2nd (GD)
8MB	AKE3EFPKN01	AKE3E100Q00	AKE3EFP0N07	AKE2EZN0Q00
16MB	AKE3DZKN00	AKE2DF0KQ00	AKE3DZN0N01	AKE3DF00Q00
Socket	DFHS08FS046			

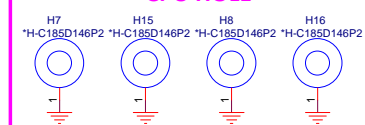
## PCH SPI ROM(CLG)

PCH 6\*5mm WSON 16M  
SPI ROM SocketEC 6\*5mm WSON 8M  
SPI ROM Socket

## OTHERS



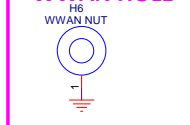
## CPU HOLE



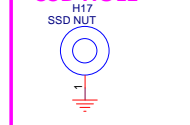
## WLAN HOLE



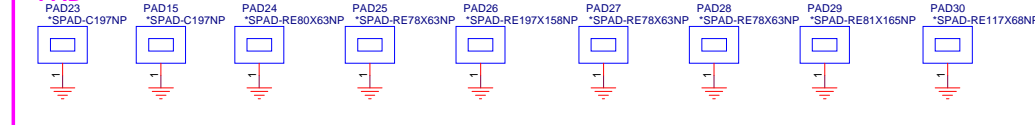
## WWAN HOLE



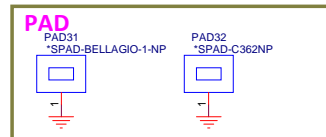
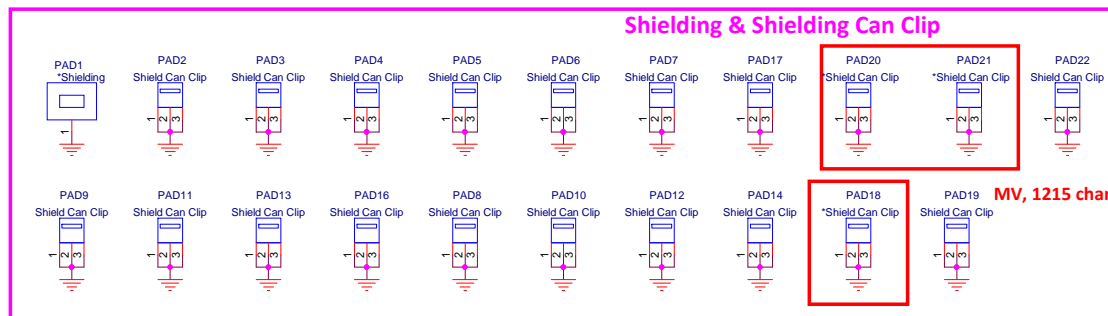
## SSD HOLE



## PAD

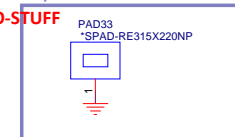


## Shielding &amp; Shielding Can Clip

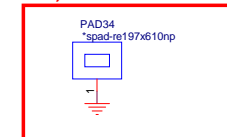


SI1, 0422 ADD

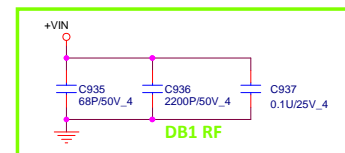
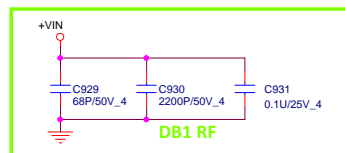
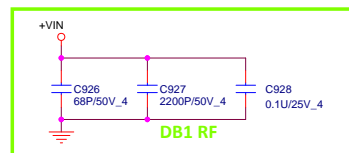
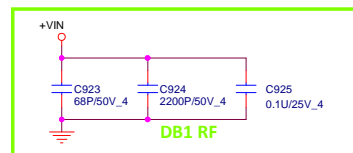
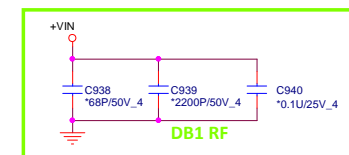
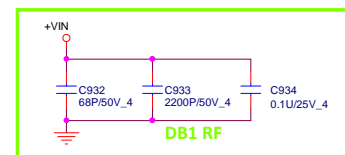
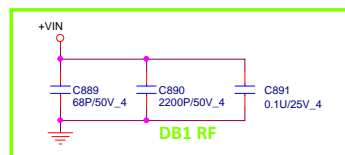
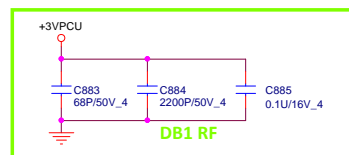
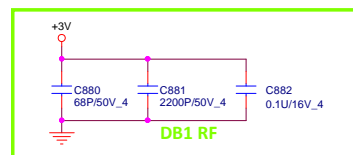
PV, 0915 ADD

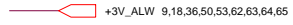


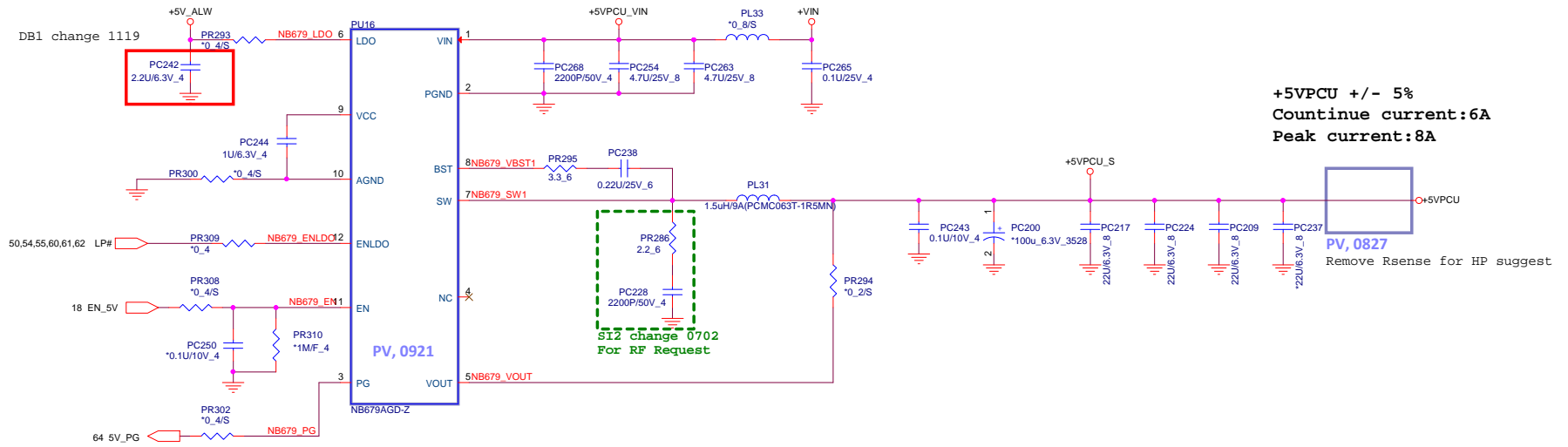
PVR, 1021 ADD



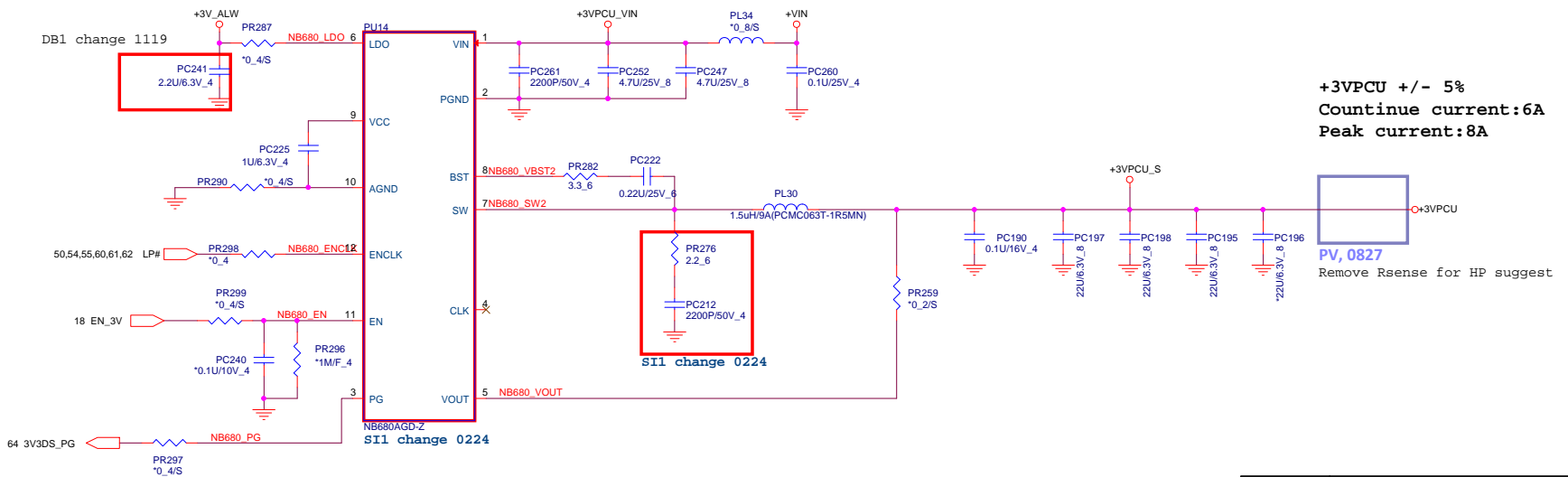
MV, 1215 change to NO-STUFF







**+5VPCU +/- 5%**  
**Countinue current:6A**  
**Peak current:8A**



**+3VPCU +/- 5%**  
**Countinue current:6A**  
**Peak current:8A**



20,44,48,49,50,51,53,54,55,57,58,59,60,61,66 +VIN  
 9,18,36,49,50,53,62,63,64,65 +3V\_ALW  
 9,10,15,55,62,65 +1.0V\_DEEP\_SUS  
 +3VPCU  
 10,21,22,24 +1.5V

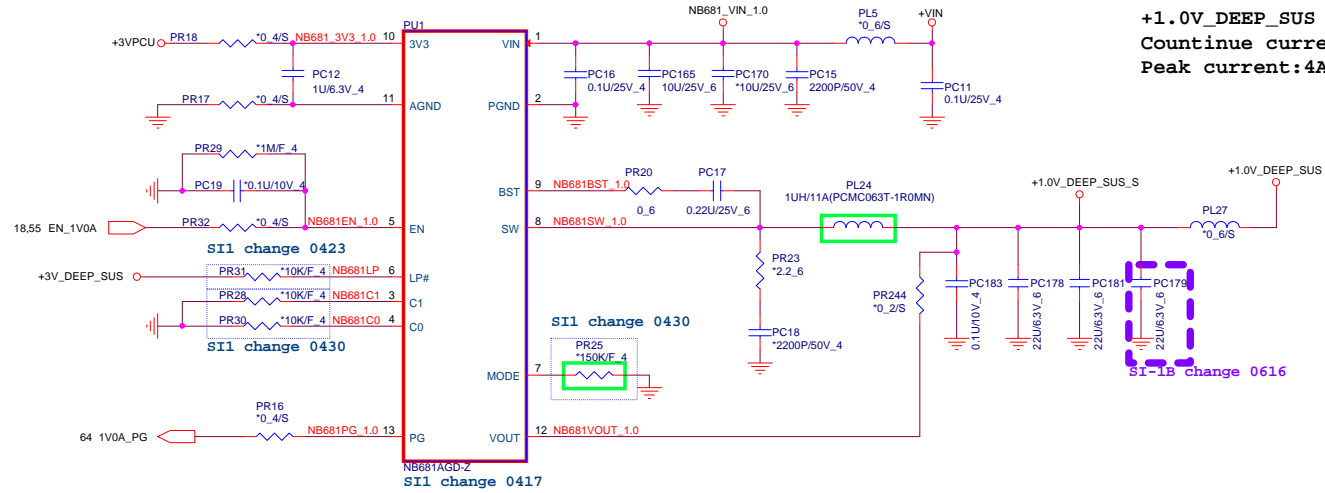
## VCC\_PRIM

LP#	C1	C0	Vout
0	X	X	0.7
1	0	0	0.8
1	0	1	0.9
1	1	0	0.95
1	1	1	1.0

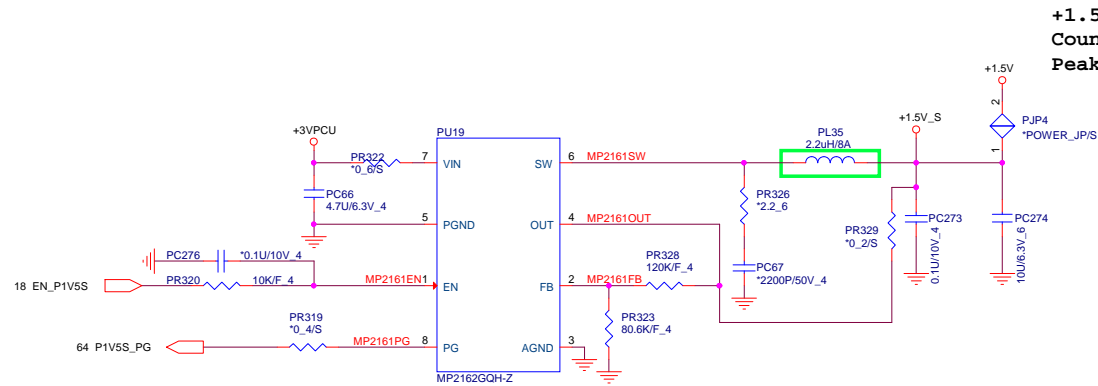
## MODE

	VR rail	Resistor
M1	VCCIO	0
M2	PRIMCORE	Float
M3	EDRAM/EOPPIO	100K
M4	other	150K

54,65 LOW\_PWR\_VTG\_SHIFT PR26 \*0.4/P NB681C0  
 51,53,54,55,65 LOW\_PWR\_VTG\_SHIFT\_N PR27 \*0.4/P NB681C1

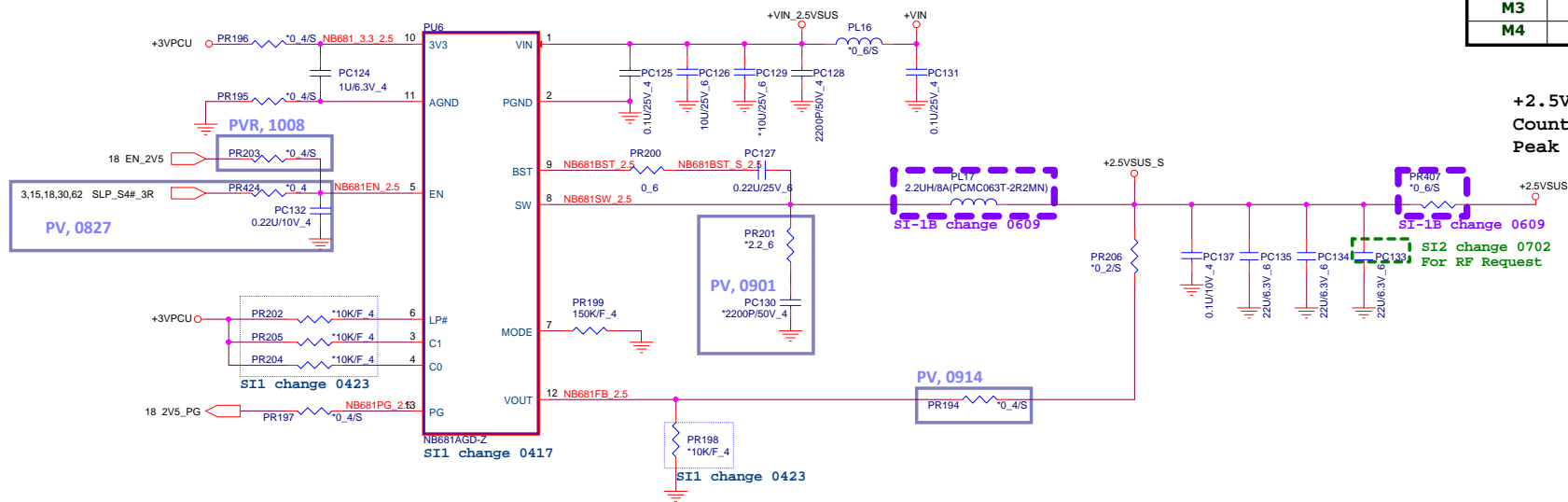
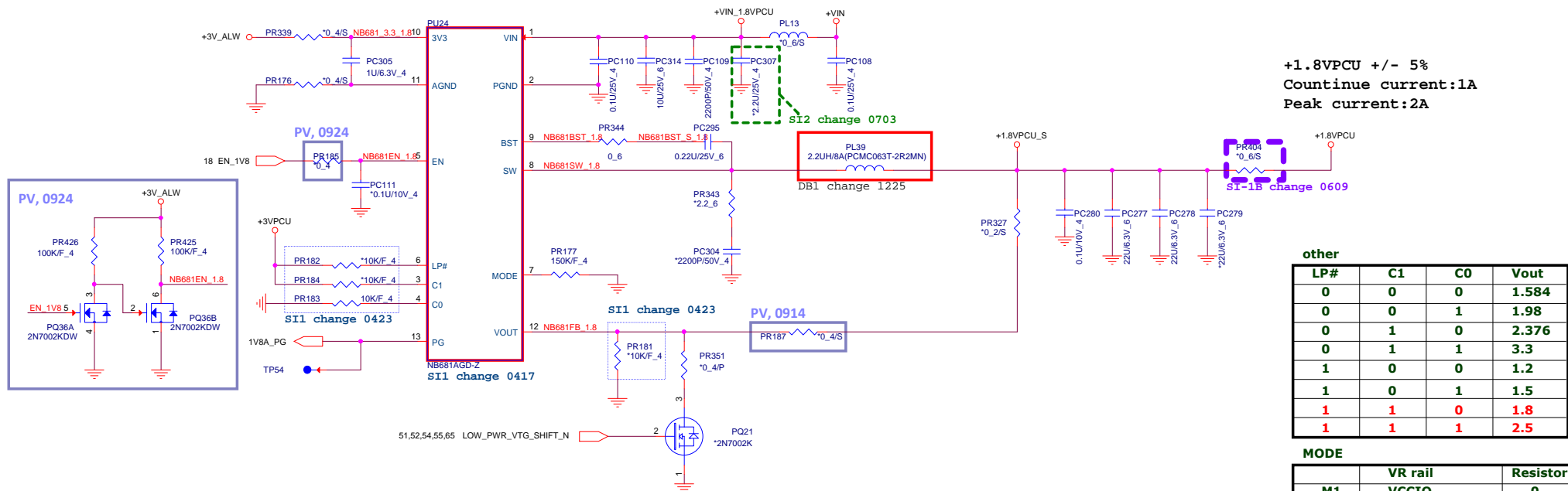


+1.0V\_DEEP\_SUS +/- 5%  
 Countinue current:2A  
 Peak current:4A

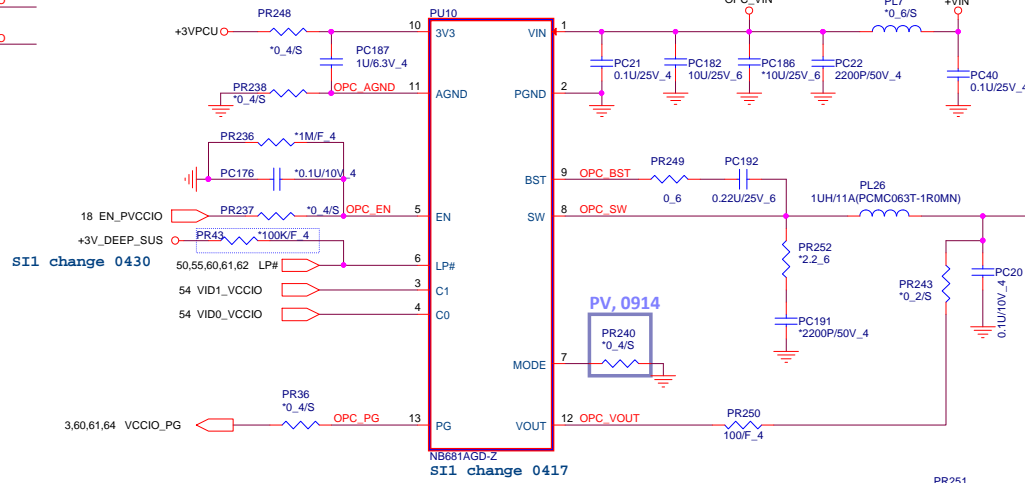
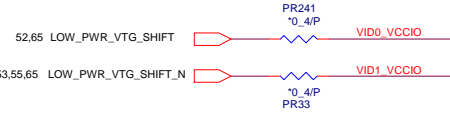
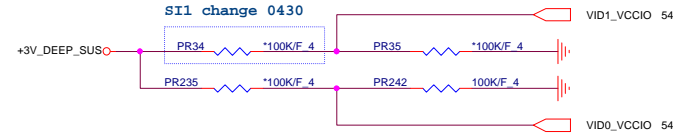


+1.5V +/- 5%  
 Countinue current:1A  
 Peak current:2A





20,44,48,49,50,51,52,53,55,57,58,59,60,61,66 +VIN  
9,18,36,49,50,53,62,63,64,65 +3V\_ALW  
5,13,15,38 +VCC\_IO



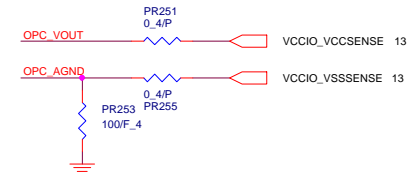
+VCC\_IO +/- 5%  
Countinue current:2A  
Peak current:3A

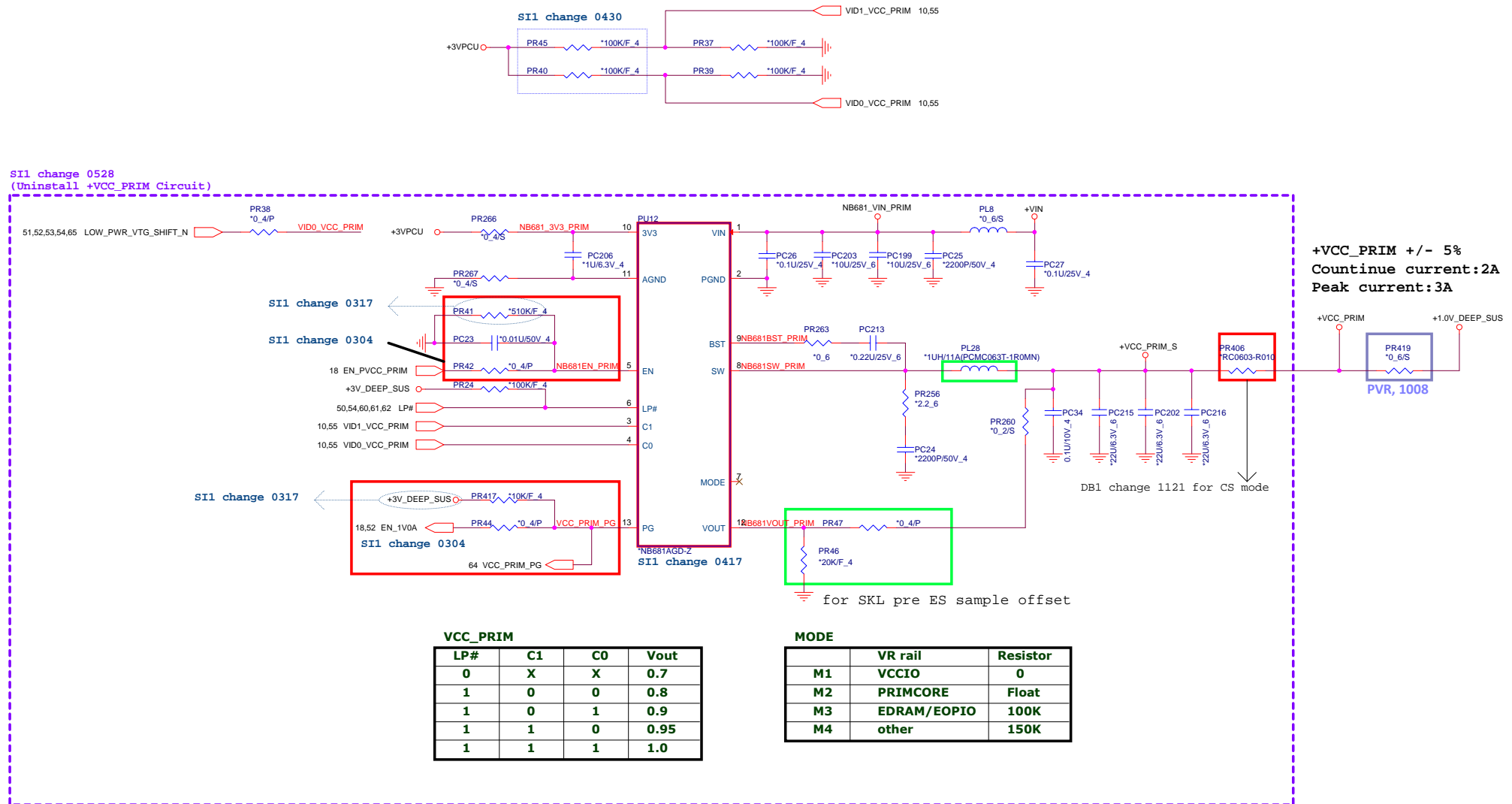
#### VCCIO

LP#	C1	C0	Vout
0	X	X	0
1	0	0	0.85
1	0	1	0.875
1	1	0	0.95
1	1	1	0.975

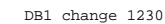
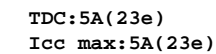
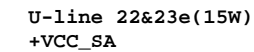
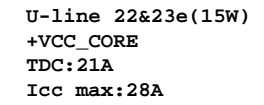
#### MODE

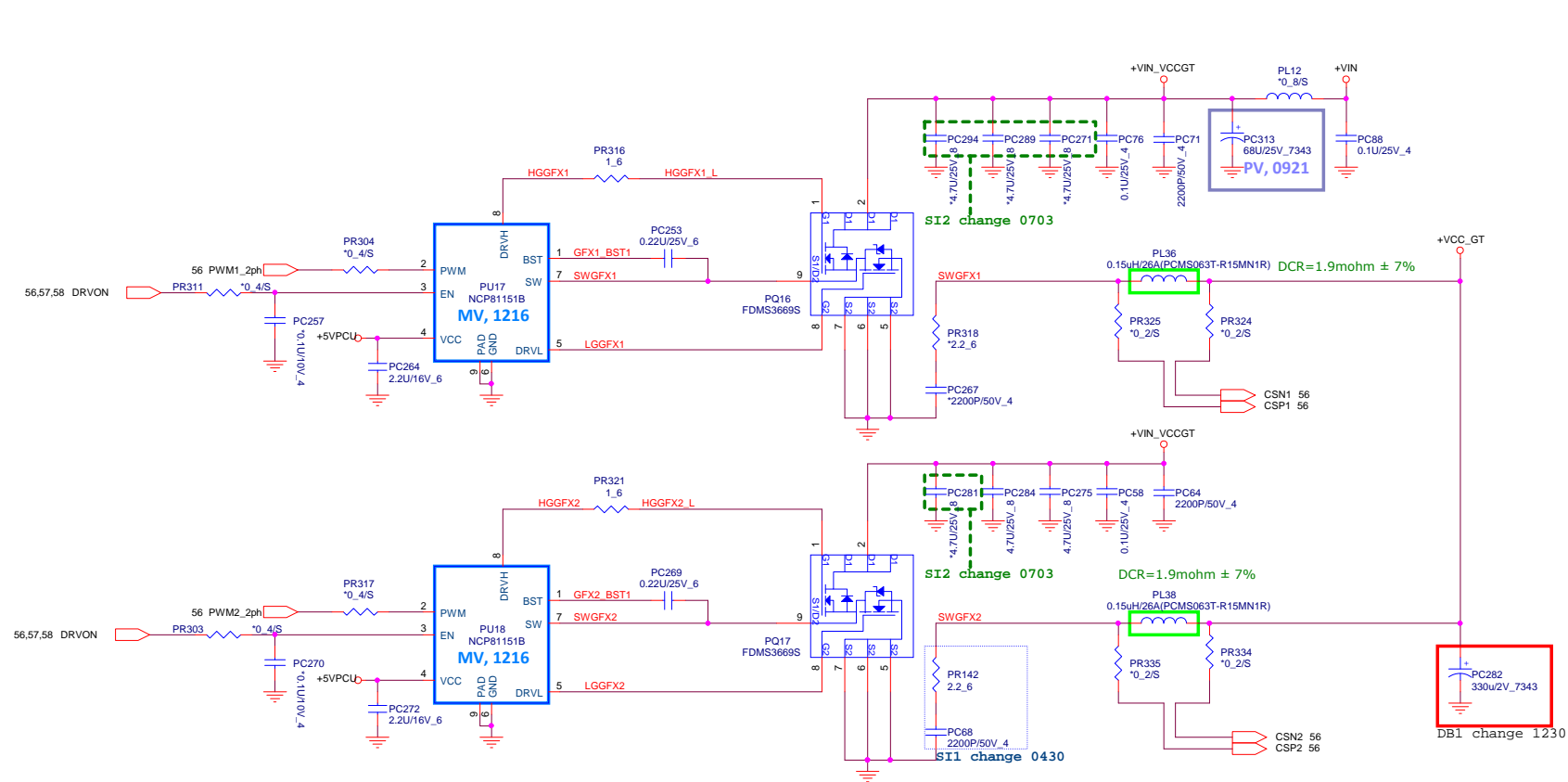
	VR rail	Resistor
M1	VCCIO	0
M2	PRIMCORE	Float
M3	EDRAM/EOPPIO	100K
M4	other	150K







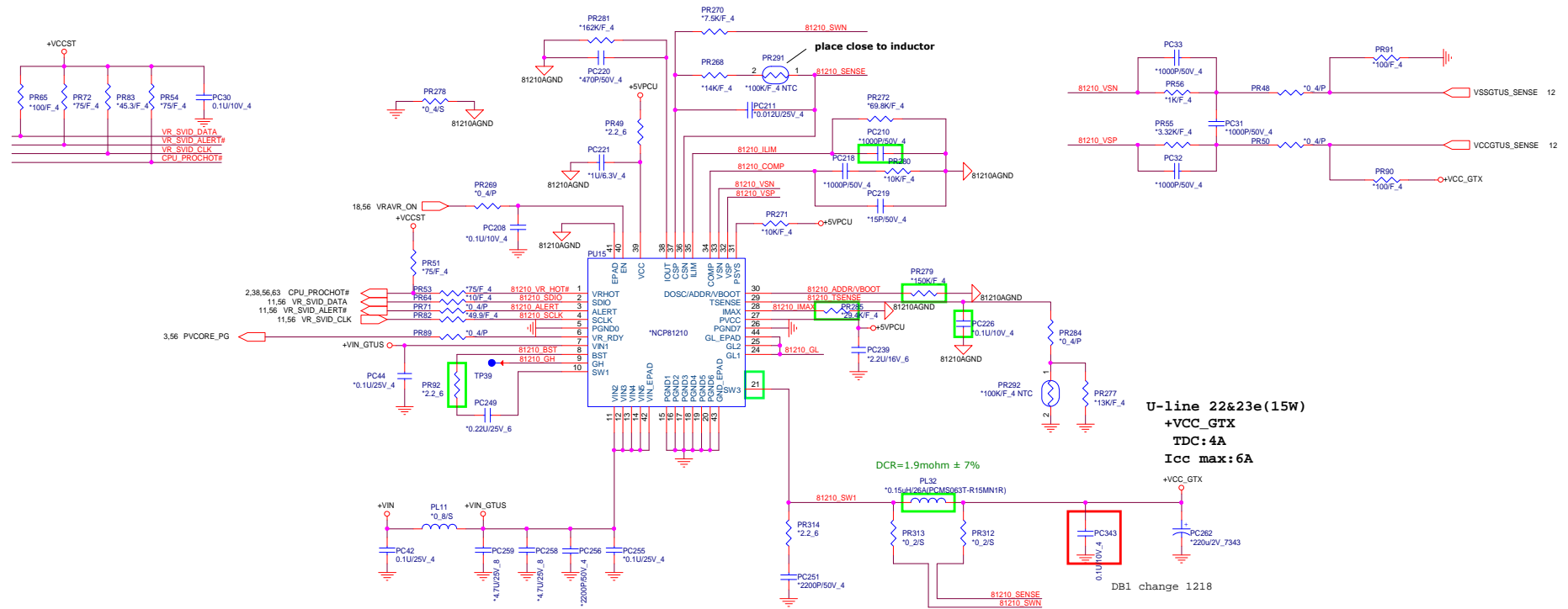




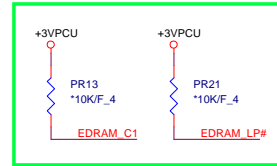
U-line 22&23e(15W)  
+VCC\_GT

```
TDC:18A(22)
Icc max:31A(22)
```

TDC: 32A(23e)  
Icc max 56A(23e)



for SKL pre ES sample

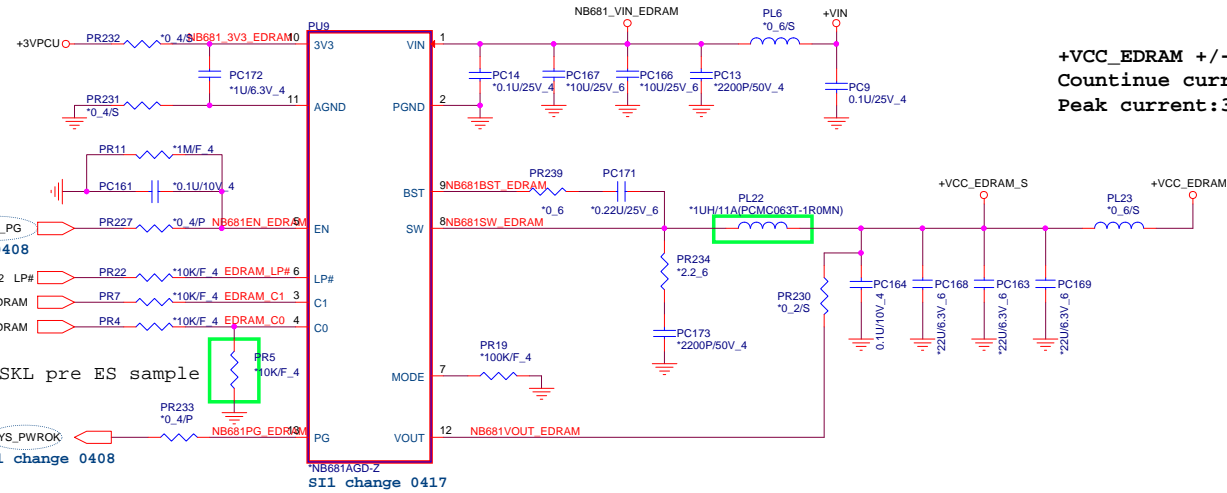


3,54,61,64 VCCIO\_PG  
SII change 0408

50,54,55,61,62 LP#  
11 VID1\_VCC\_EDRAM  
11 VID0\_VCC\_EDRAM

for SKL pre ES sample

3,61 SYS\_PWROK  
SII change 0408



+VCC\_EDRAM +/- 5%  
Countinue current:2A  
Peak current:3A

VCC\_EDRAM

LP#	C1	C0	Vout
0	X	X	0
1	0	0	0.8
1	0	1	0.95
1	1	0	1.0
1	1	1	1.05

MODE

	VR rail	Resistor
M1	VCCIO	0
M2	PRIMCORE	Float
M3	EDRAM/EOPPIO	100K
M4	other	150K



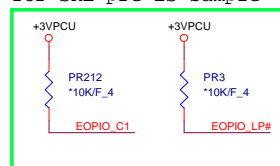
PROJECT : Y0F  
Quanta Computer Inc.

Size	Document Number +VCC_EDRAM (NB681)_23E	Rev 1A
Date: Tuesday, December 22, 2015 Sheet 60 of 67		



20,44,48,49,50,51,52,53,54,55,57,58,59,60,66 +VIN  
9,18,36,49,50,53,62,63,64,65 +3V\_ALW  
11 +VCC\_EOPIO

for SKL pre ES sample



3.54,60,64 VCCIO\_PG  
SII change 0408

for SKL pre ES sample

3.60 SYS\_PWROK  
SII change 0408

50,54,55,60,62 LP#  
11 VID1\_VCC\_EOPIO  
11 VID0\_VCC\_EOPIO

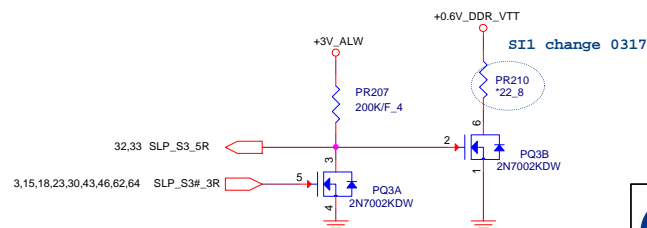
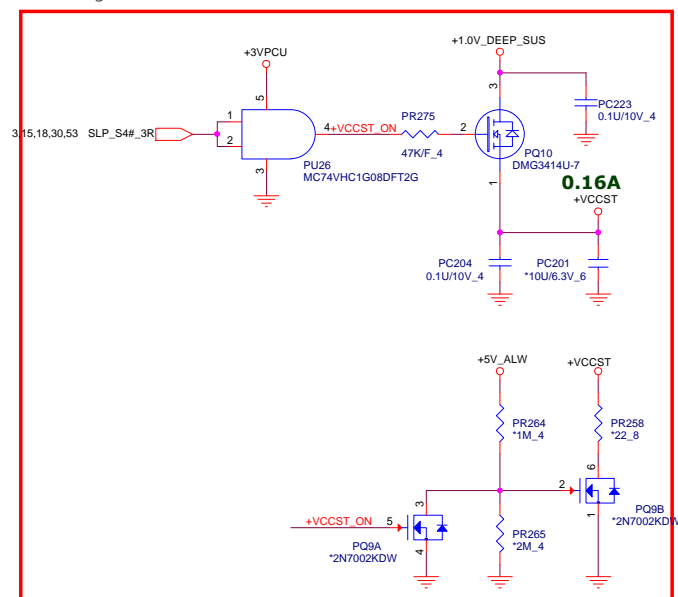
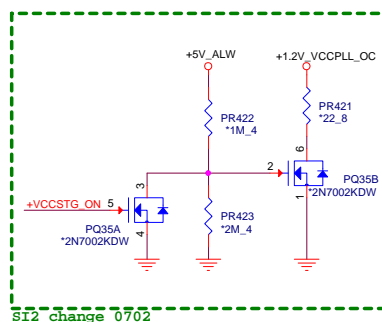
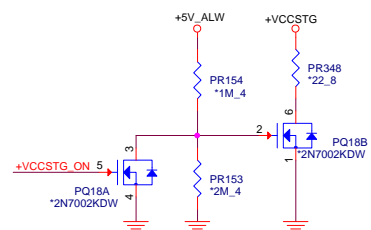
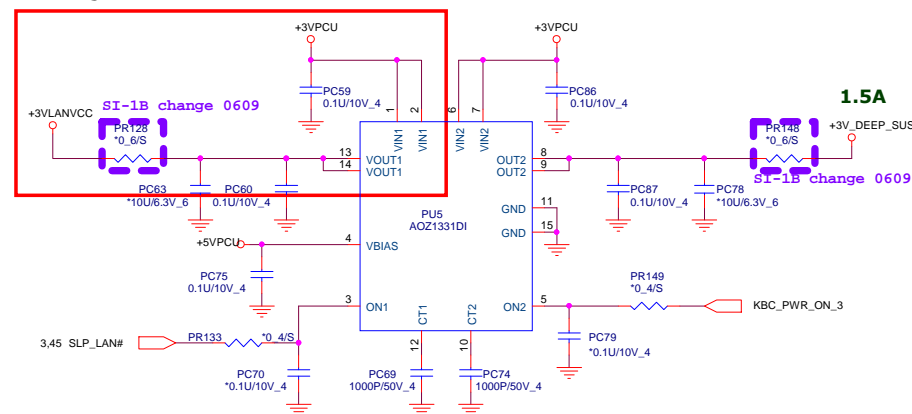
#### VCC\_EOPIO

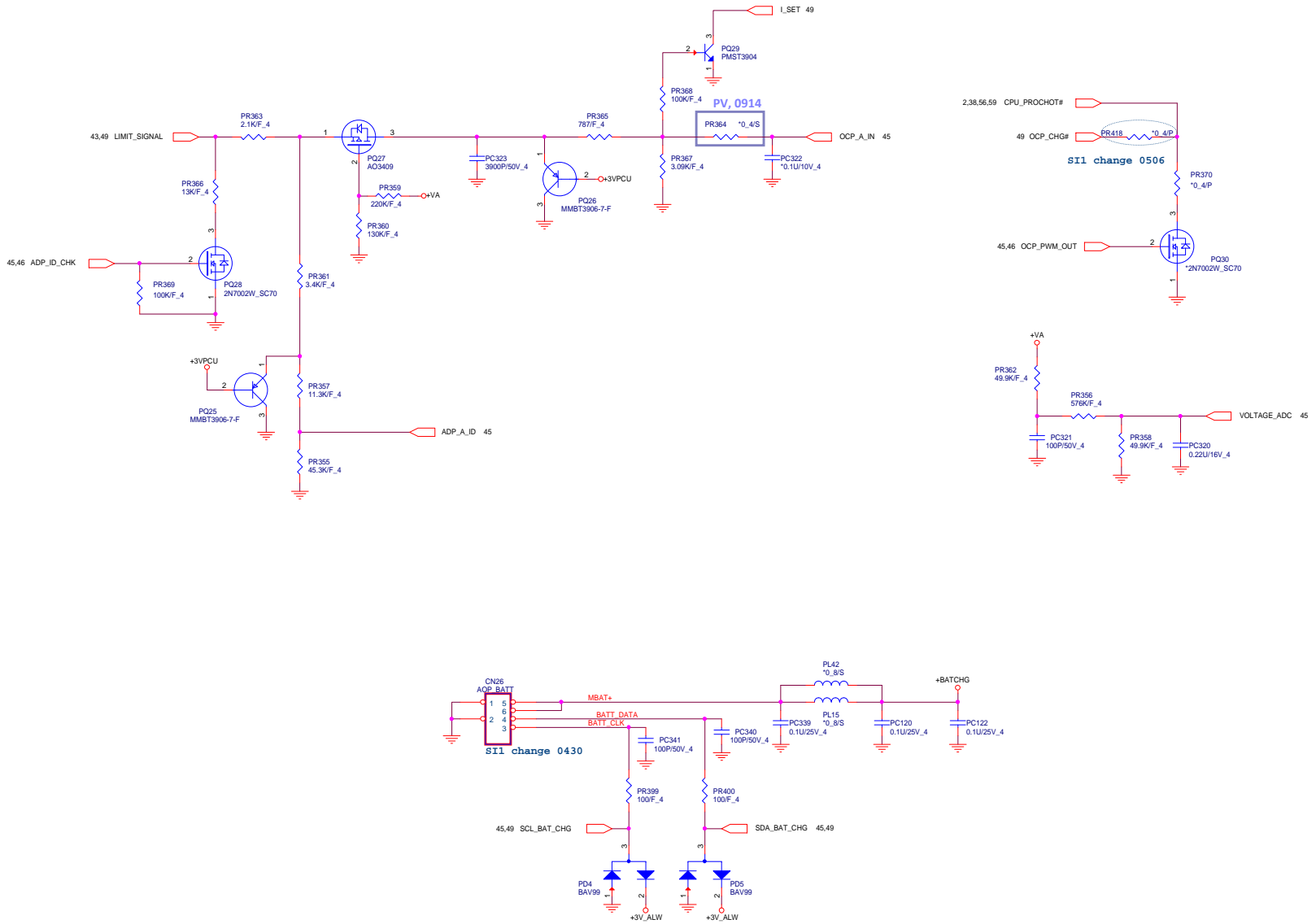
LP#	C1	C0	Vout
0	X	X	0
1	0	0	0.8
1	0	1	0.95
1	1	0	1.0
1	1	1	1.05

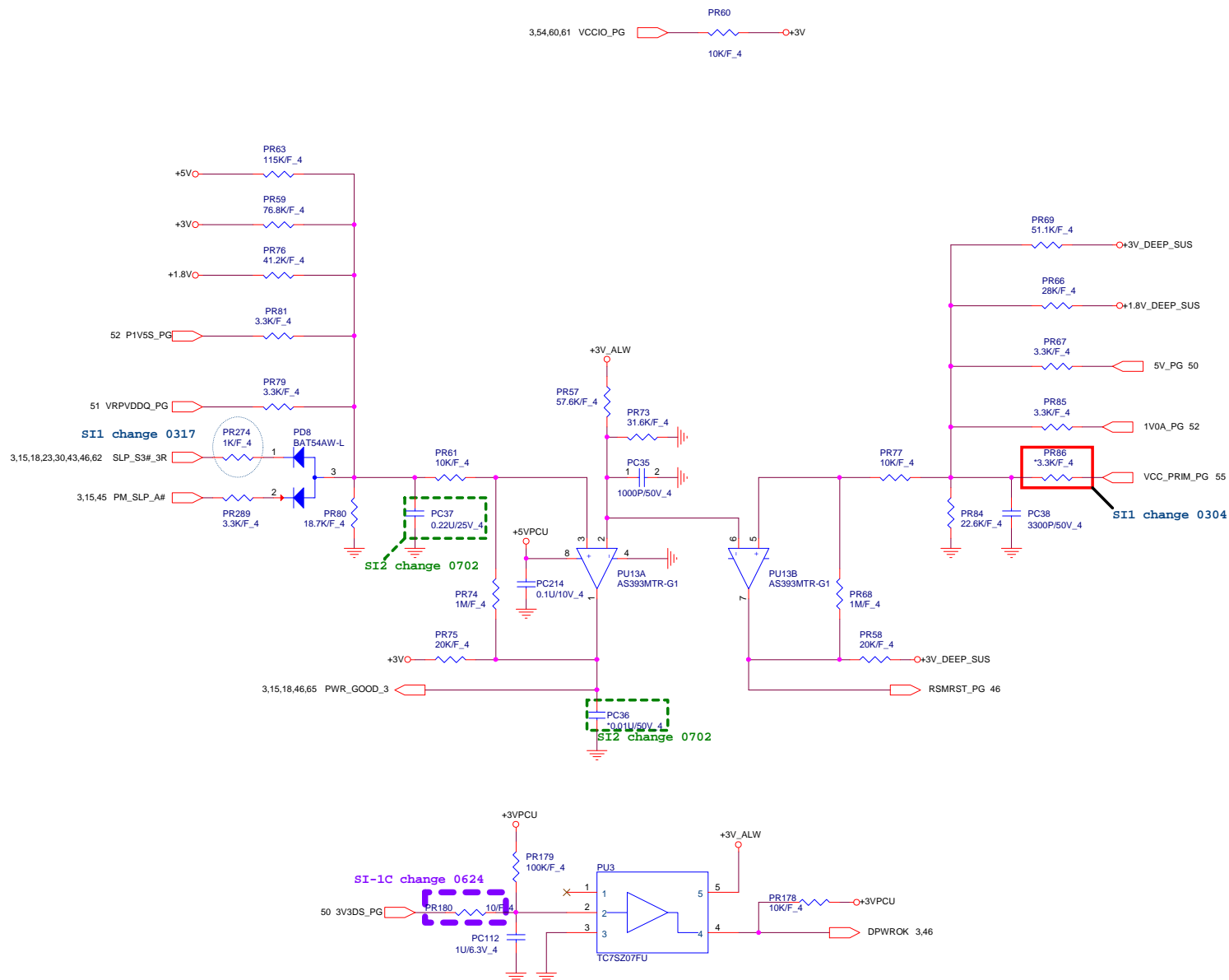
#### MODE

	VR rail	Resistor
M1	VCCIO	0
M2	PRIMCORE	Float
M3	EDRAM/EOPIO	100K
M4	other	150K

+VCC\_EOPIO +/- 5%  
Countinue current:2A  
Peak current:3A







**PROJECT : Y0F**  
**Quanta Computer Inc.**

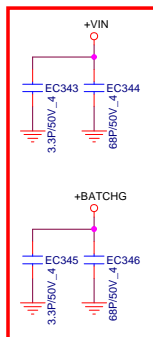
Size Custom	Document Number <b>Power OK</b>	Rev 1A
Date: Tuesday, December 22, 2015	Sheet 64 of 67	

2,3,4,5,7,8,9,10,15,19,20,21,22,24,27,28,29,37,38,39,40,44,45,48,49,56,62 +3V  
 8,20,24,25,27,34,35,39,62,85 +5V  
 9,18,36,49,50,53,62,63,65 +3V\_ALW

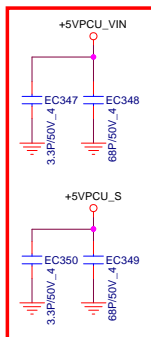


**Charger**

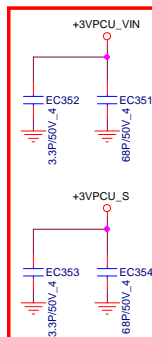
SI1 change 0224

**+5VPCU**

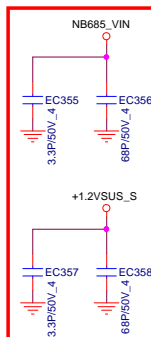
DB1 change 1222

**+3VPCU**

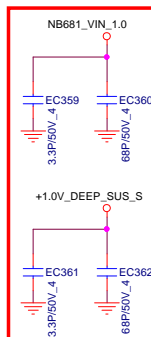
DB1 change 1222

**+1.2VSUS**

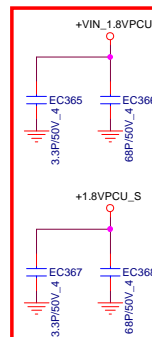
DB1 change 1222

**+1.0V\_DEEP\_SUS**

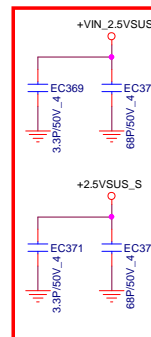
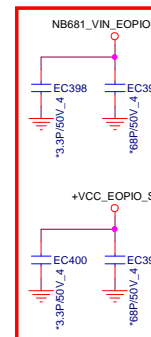
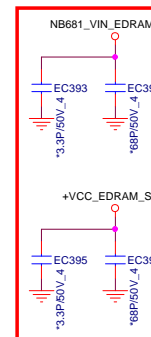
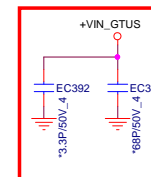
DB1 change 1222

**+1.8VPCU**

DB1 change 1222

**+2.5VSUS**

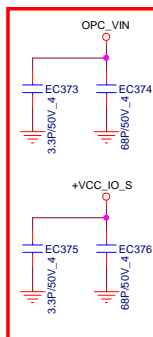
DB1 change 1222

stuff for 23e  
no stuff for 22**+VCC\_EOPIO****+VCC\_EDRAM****+VCC\_GTX**

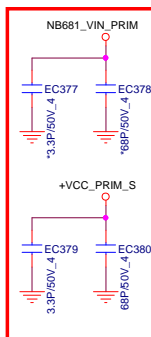
DB1 change 1223

**+VCC\_IO**

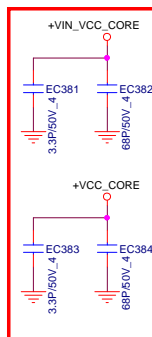
DB1 change 1222

**+VCC\_PRIM**

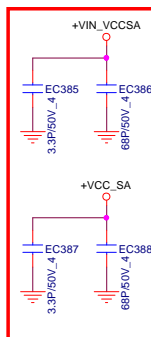
DB1 change 1222

**+VCC\_CORE**

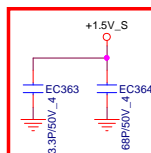
SI1 change 0224

**+VCC\_SA**

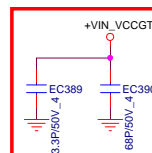
DB1 change 1222

**+1.5V**

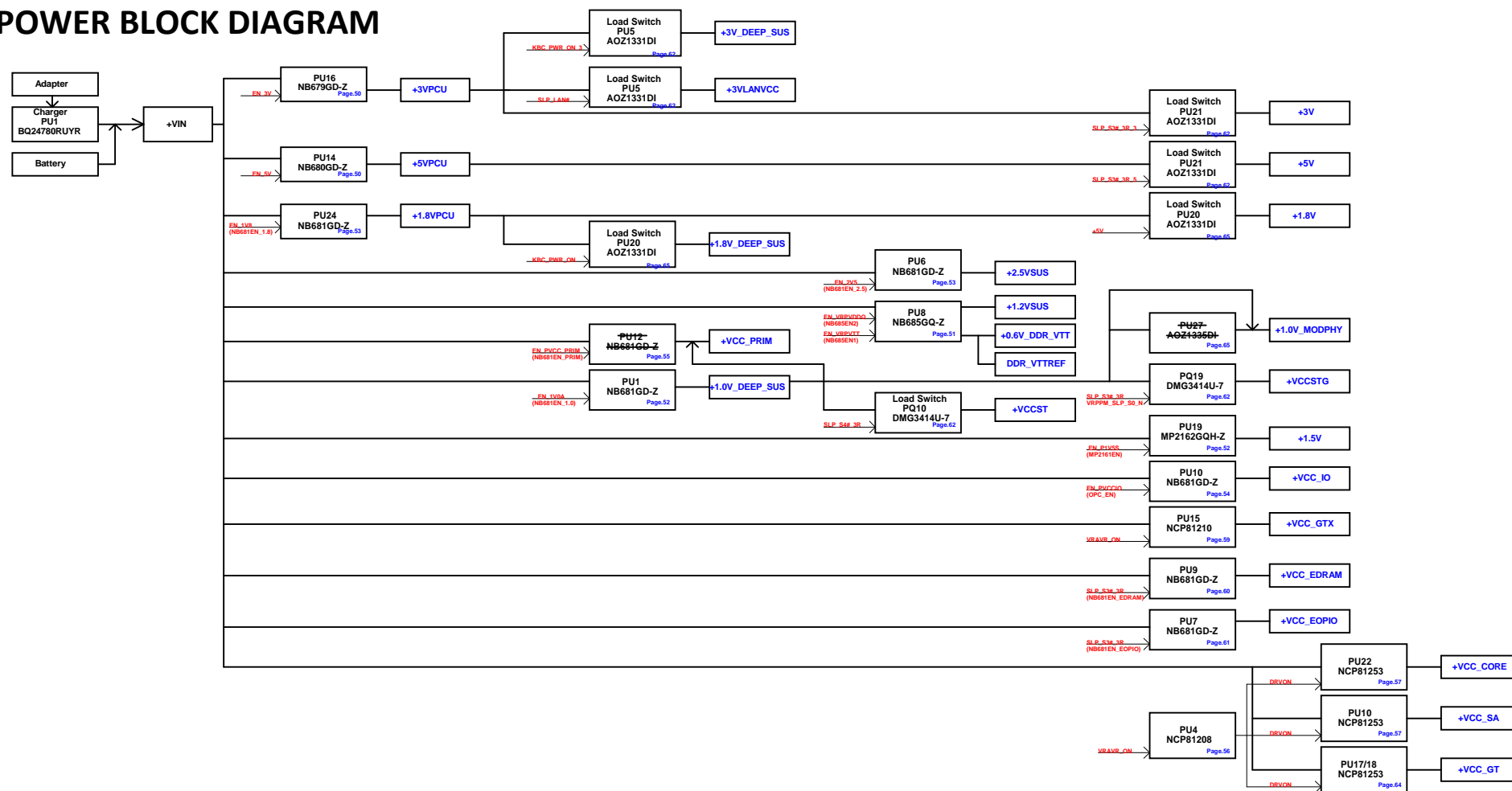
DB1 change 1222

**+VCC\_GT**

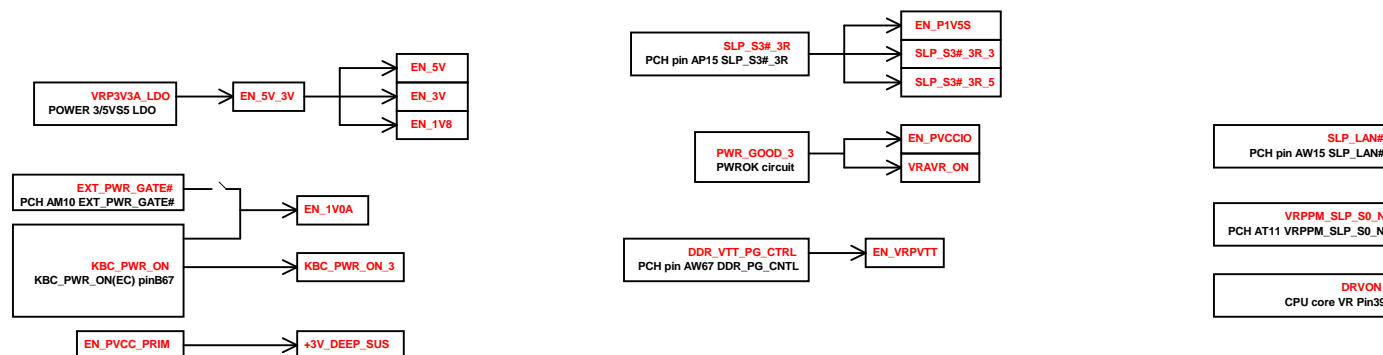
DB1 change 1222

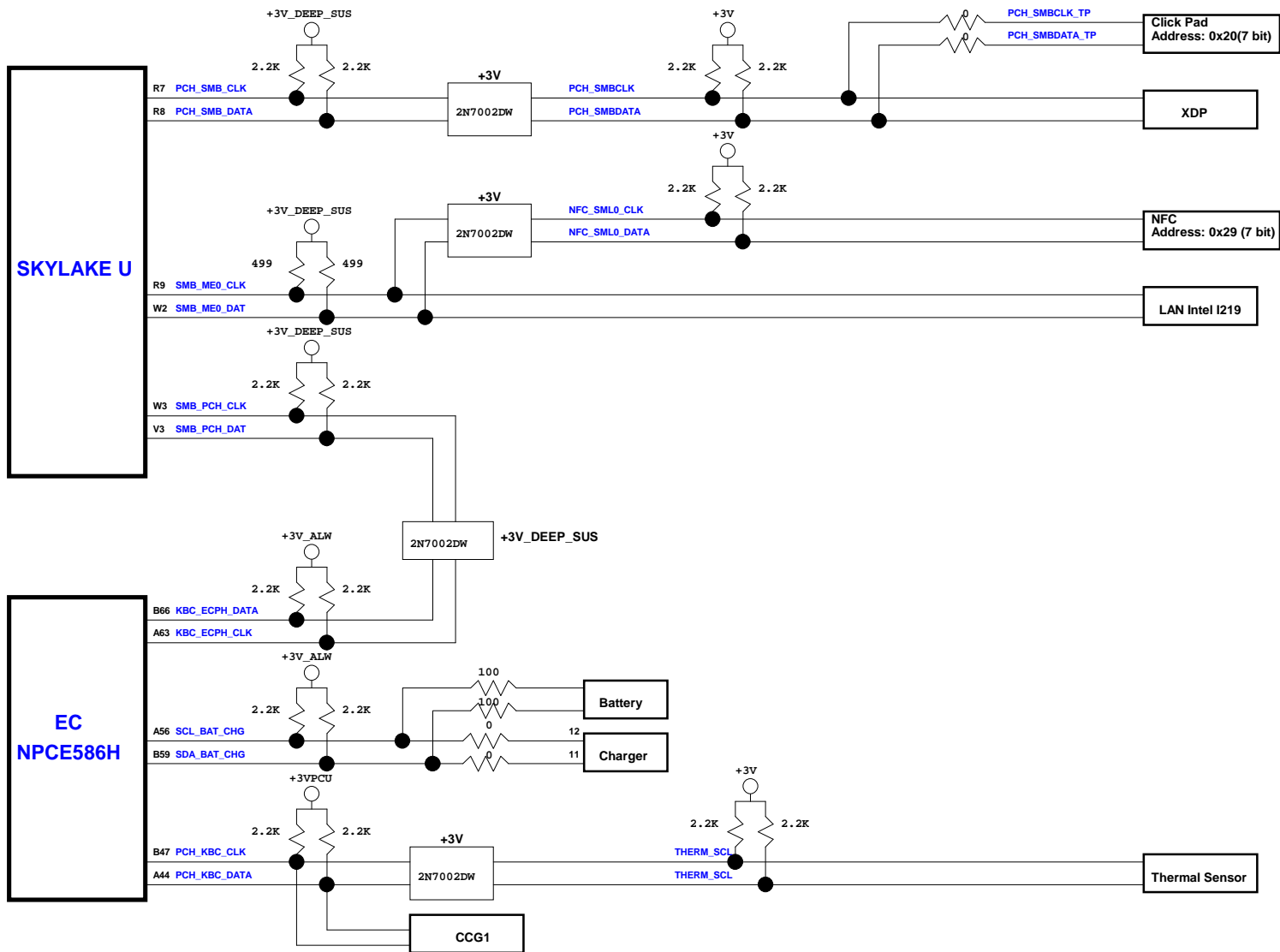


# POWER BLOCK DIAGRAM



## POWER ENABLE PIN





Multiplexed HSIO Lane	Port Assignment
USB3 #1	USB2.0/USB3.0 Combo Jack(Right side)
USB3 #2 / SSIC #1	USB2.0/USB3.0 Combo Jack(Left side)
USB3 #3 / SSIC #2	USB3.1 (Type-C)
USB3 #4	USB3.0 Dock
PCIE1 / USB3 #5	USB3.1 (Type-C)
PCIE2 / USB3 #6	NC
PCIE3	LAN
PCIE4	WLAN
PCIE5	NC
PCIE6	NC
PCIE7 / SATA #0	NC
PCIE8 / SATA #1	NC
PCIE9	SSD (SATA)
PCIE10	SSD (SATA)
PCIE11 / SATA #1*	SSD (SATA)
PCIE12 / SATA #2	SSD (SATA)

USB2.0	Port Assignment
USB2 #1	USB2.0/USB3.0 Combo Jack(Right side)
USB2 #2	USB2.0/USB3.0 Combo Jack(Left side)
USB2 #3	WWAN
USB2 #4	USB2.0(Dock)
USB2 #5	USB2.0(Type-C)
USB2 #6	NC
USB2 #7	Bluetooth
USB2 #8	Finger Print
USB2 #9	Camera
USB2 #10	SmartCard